**Digital Watermark and Fingerprint in Variable Rank Linear-Feedback Shift Register.**

**A. A. Ivaniuk 1**

**V. V. Sergeichik**

 1 Белорусский государственный университет информатики и электроники

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**Abstract:** This paper presents new watermarking approach for hardware IP-core (Intellectual Property core) protection. The approach operates in BIST’s (Built-In Self-Test) test pattern generation circuit—Variable Rank Linear-Feedback Shift Register (VR-LFSR), therefore it has wide application area. Theoretical part surveys related work, outlines the approach, studies attack resilience and probability of coincidence. Experimental part explores hardware implementations and their overheads. Fingerprinting approach, which can be used simultaneously with watermarking, is presented.

**Keywords:** IP-core protection, IP-watermarking, IP-fingerprinting, dynamic watermark.

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