**Low read-only memory distributed arithmetic implementation of quaternion multiplier using split matrix approach**

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**Abstract.** In most algorithms that use quaternion numbers, the key operation is a quaternion multiplication, of which the efficiency and accuracy obviously determine the same properties of the whole computational scheme of a filter or transform. A digit ( L -bit)-serial quaternion multiplier based on the distributed arithmetic (DA) using the splitting of the multiplication matrix is presented. The circuit provides the facility to compute several products of quaternion components concurrently as well as to reduce the memory capacity by half in comparison with the known DA-based multiplier, and it is well suited for field programmable gate array (FPGA)-based fixed-point implementations of the algorithms. Apart from a theoretical development, the experimental design results which are obtained using a Xilinx Virtex 6 FPGA are reported.

**Keywords:**

INSPEC: Controlled Indexing read-only storage, distributed arithmetic, field programmable gate arrays, matrix algebra.

INSPEC: Non-Controlled Indexing.

ROM, Xilinx Virtex 6 FPGA, field programmable gate array, DA-based multiplier, multiplication matrix, quaternion multiplication, split matrix, quaternion multiplier, distributed arithmetic.

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