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Oxidized Porous Silicon: From Dielectric Isolation to Integrated Optical Waveguides

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Abstract. A brief review of 20-years research of formation, processing and utilizing of oxidized porous silicon (OPS) is presented. Electrolytes to form porous silicon (PS) layers, special features of PS chemical cleaning and thermal oxidation are discussed. OPS application for dielectric isolation of components of bipolar ICs and for the formation of silicon-on-insulator structures has been demonstrated. Although these OPS-based techniques have found limited current commercial use, experience gained is applicable to the fabrication of optoelectronic devices. Specifically, integrated optical waveguides based on OPS have been developed.

Keywords: oxidized porous silicon, anodization, oxidation, dielectric isolation, optical waveguide

1. Introduction

Oxidation of porous silicon (PS) has been being turned to practical use since 1969 when NTT and Sony Corporations patented the dielectric isolation of components of microelectronic devices by OPS [1, 2]. The patented method was named IPOS (Isolation by Porous Oxidized Silicon). In the IPOS method, local OPS regions have isolated the components of ICs from each other in lateral direction, while p-n junction has provided the isolation from the substrate [3]. A variety of IPOS modifications (n^+-type IPOS, p-type IPOS, etc.) have been developed as a possible alternative to isolation by p-n junction, LOCOS and Isoplanar methods.

Beginning in 1977, Integral Corporation (Minsk, Belarus) with the participation of Minsk Radioengeneering Institute started the employment of IPOS technology for bipolar ICs. The IPOS processes for epitaxial structures with the thickness of from 1.5 to 10 μm on both p-type and n^+-type substrates have been developed [4, 5]. When oxidation of Si under high pressure has been mastered, Isoplanar technique for bipolar ICs and LOCOS for MOS ICs came to the forefront in industrial production. However, IPOS remains the only means to provide deep SiO_2 regions with the thickness of 5–10 μm for dielectric isolation of high-voltage bipolar devices.

The original methods of silicon-on insulator (SOI) structure formation have inspired a renewed interest in OPS. A variety of techniques for manufacturing SOI structures based on OPS layers have been invented [6–10]. A method favored by our group has been based on preferential anodization of n^+-layer within $n^-/n^+/n^-$ structure [11–13]. Notable results have been obtained by Integral Corporation [14–16]. Rad-hard high-speed logic CMOS ICs were commercially manufactured.

Discovery of intensive visible photoluminescence of PS at room temperature by Canham in 1990 have regenerated interest in PS based technologies. The totality of our experience on PS formation and processing can be useful in production of optoelectronic components and their integration with electronic components on-chip [15–17]. We have applied our experience in this

field to development of optical waveguide (WG) based on OPS [18–20].

The objective of this paper has been to present a brief overview of results we have obtained during 20 years of PS research with respect to OPS.

2. Technology of Oxidized Porous Silicon

Technological process of OPS formation has consisted of three main steps: (i) the anodic treatment of Si in HF-containing electrolyte to convert silicon into the porous state; (ii) the chemical cleaning of PS; (iii) the thermal oxidation of PS. The technological aspects of each step have been developed to succeed in OPS based technology.

Several principal problems have been solved in the way from fundamental research of PS to industrial technology of OPS. Development of any new process at a high-technology electronic company needs equipment suited to operate under clean room conditions. So, the first major task has been to design suitable equipment for the formation of PS layers of uniform thickness and porosity. It has been also necessary to develop the methods of chemical cleaning as well as defect-free oxidation of 1–10 μm thick PS layers.

2.1. Formation of Porous Silicon

A variety of electrolytes can be used to form PS layers. However, hydrofluoric acid (HF) is the main component of any electrolyte.

HF-H_2O. HF concentration in water solutions has been 5–48% depending on required PS properties. Undoped polysilicon or Si_3N_4 films have been usually used as a mask for formation of local PS regions. Small amount of surface-active substance can be added to electrolyte to provide H_2 bubbles desorption from the Si wafer surface during the anodization process [4, 5].

HF-ethylenglycol. The use of ethylenglycol as a solvent has resulted in an increase of electrolyte viscosity and hindering diffusion processes in the electrolyte. Such electrolytes have been suitable for the formation of highly porous PS layers. One of the main advantages of such electrolytes has been the possibility of using SiO_2 film as a mask [4]. Highly viscous electrolytes should be intensively stirred to provide effective removing of H_2 bubbles.

HF-isopropanol. This type of electrolyte has been developed from Bomchil et al. recommendations [21] for the formation of uniform PS layers within regions of the complicated configuration, especially for SOI structures [22].

2.2. Chemical Cleaning of Porous Silicon

The problem of PS cleaning was crucial at the beginning of our PS research. It has been essential that PS should be cleaned to an extent that it could be processed using industrial equipment and pilot lines. Moreover, utilizing PS layers in microelectronic devices has required their high purity. So, the influence of various chemical treatments on the composition of PS and properties of OPS has been studied. A comprehensive investigation using Auger electron spectroscopy (AES), secondary-ion mass spectroscopy (SIMS), and neutron activation analysis (NAA) has conclusively shown that PS layers do not produce extra contamination and can be used for device production [5].

To determine chemical solutions suitable for PS chemical cleaning, the processing of PS in standard solutions developed by RCA for Si cleaning as well as rinsing in de-ionized water has been examined. Solutions based on H_2O_2-NH_4OH-H_2O have been totally unsuited for PS treatment since they have been harmful towards PS. With evidence provided by SIMS and NAA, the cleaning of PS has been best achieved by rinsing in de-ionized water for 20–25 min, boiling in the solution based on H_2O_2-HCl-H_2O (1 : 1: 3) for 10–15 min, and rinsing in de-ionized water for 20–25 min, in succession. It has been determined that the rinsing in de-ionized water should be performed immediately after PS formation. Once chemical cleaning has been performed, PS should be oxidized as quickly as possible.

2.3. Thermal Oxidation of Porous Silicon

Due to the large surface/volume ratio, PS has a very high rate of oxidation. This has allowed the oxidation of thick porous layers in a short time. However, when heated to temperature higher than 500°C, PS has undergone irreversible transformations in the original microstructure (sintering) [23, 24]. The sintering has prevented the PS layer from the oxidation. It can be easily avoided by pre-oxidation of PS electrochemically or thermally at low ∼300°C temperature in dry oxygen. Temperatures 800–900°C have been used to

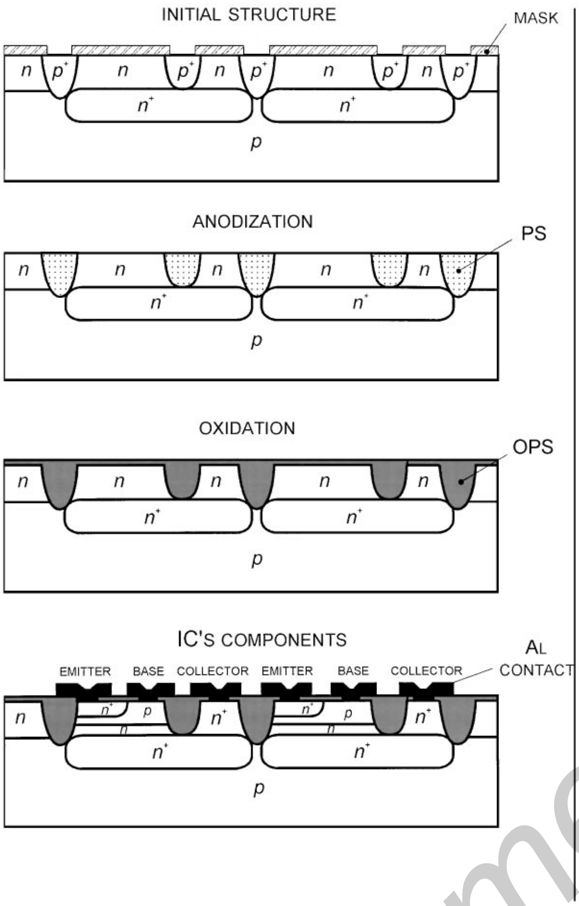

Figure 1. Application of IPOS technology for bipolar ICs.

oxidize PS. However, the quality of the material obtained has been still very different from that of standard thermal SiO_2. A densification step at 1050–1150°C in wet oxygen followed by annealing in nitrogen has been necessary to form an OPS equivalent to thermal SiO_2. Very good results have been obtained using oxidation in oxygen under high pressure at 800–950°C followed by annealing in nitrogen at 1150–1200°C.

Both electrical and optical characteristics of OPS have strongly depended on PS porosity and oxidation regimes. Dielectric properties of OPS provided by the optimum process have been found to be very close to that of thermal SiO_2 [4, 5, 22].

3. Isolation by Oxidized Porous Silicon

The main application of IPOS method has been bipolar ICs as illustrated in Fig. 1. The prime function of OPS regions has been to isolate the components of ICs from each other in lateral direction. We have succeeded in p-type and p^+-type IPOS techniques and modified n^+-type IPOS. In the first method, local regions of p-type epitaxial layer have been anodized in electrolyte containing HF and glycol through mask openings. Since the epitaxial layer has been doped with boron uniformly, there has been no problem of uneven porosity. Our main concern has been to determine both optimal anodization regimes to provide porosity of ~56% and regimes of PS oxidation. The structures with the epitaxial layer thickness of ~0.8–3 μm have been utilized to fabricate high speed bipolar VLSI [4]. In the second technique, p^+-type silicon regions doped with boron have been anodized. These regions have had a concentration gradient of dopant in both vertical and lateral directions [5]. The uniform porosity of PS layers in this case has been more difficult to attain, especially for ~8–10 μm thick PS layers. Such structures have been of use as a base for fabrication of high voltage bipolar ICs. In the third method, n^+-type regions doped with phosphorus have been anodized. Since the non-uniform allocation of dopant throughout the volume of n^+-type regions has occurred, a search for optimal regimes of anodic treatment has been of prime importance. The n^+-type IPOS structures with ~1–3 μm thick epitaxial layers have been utilized to fabricate bipolar microprocessor ICs.

The search for optimal regimes of OPS regions formation has been a challenging task. This has been due to the fact that PS and OPS characteristics (porosity, thickness, etc.) depend on a great number of factors. The task for uniformly doped p-type Si has been solved by method of multiple-factor design of experiments and optimization [4]. The OPS regions formed in optimized regimes have been planar and have exhibited characteristics close to those of thermal SiO_2. We have applied the optimized p-type IPOS technology for bipolar ICs production. Throughout 1978 to 1985, bipolar IC's 256-bit, 1 K and 4 K SRAM were developed. Simultaneously Isoplanar technology has been mastered. It has made possible a comparison between IPOS and Isoplanar methods. In Fig. 2 are shown the profiles of isolating regions of 2.0 μm thick formed by both technologies. IPOS technology has offered several advantages over the Isoplanar, namely:

- planarity (flatness) of isolation (absence of regions of type “bird’s beak” or “bird’s head”);
- lower width of isolating regions with the same mask opening width;

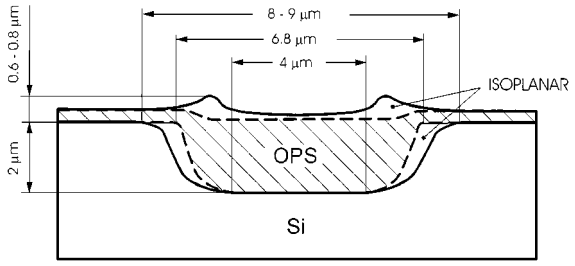

Figure 2. Profiles of isolating regions formed by Isoplanar and IPOS techniques.

— lower elastic stresses and temperature action on structures during formation of isolating regions;

At one time a number of devices has been manufactured commercially. Then the oxidation under high pressure has been developed, and Isoplanar technique for bipolar ICs and LOCOS for MOS ICs were preferred by VLSI mass production. However, Isoplanar has been unusable as a technique for the formation of deep 8–10 μm-thick isolation regions for high-voltage bipolar devices. To form them, p^+-type IPOS has been utilized. P^+-type regions have been formed by long-continued boron diffusion to a depth of 10–12 μm through the epitaxial layer. Boron diffusion has formed the p-n junction isolation within the initial Si structures. Then, two additional operations (porous anodization and thermal oxidation) have been introduced into the technological process with the resulting conversion of p^+-type regions into OPS. The galvanostatic anodization regime has failed to produce the low-defects IPOS isolation [25]. To provide the desired isolation, anodization with time dependent current has been performed. This enabled PS porosity to be controlled when thick diffusion regions have been anodically treated [26]. We have evolved the method of PS oxidation consisted of two steps. The first step has been performed by electrochemical oxidation of PS in NH_4NO_3/glycol electrolyte. Then the three-stage thermal oxidation has been performed. As a result, a thin dense layer of high-quality thermal SiO_2 has been formed at the interface with Si while the bulk of the isolation region has been occupied with porous SiO_2 of the low porosity. The layer of dense thermal SiO_2 has ensured a reliable electrical isolation. Porous SiO_2 has provided a planarity of the isolation. Moreover, a porous structure of the bulk isolation volume has allowed the formation of deep isolation regions without considerable elastic stresses even with the 8–10 m thickness. This technology has been used to produce bipolar high-voltage ICs for automotive and television equipment.

Structures with modified n^+-type IPOS have been utilized for bipolar I^2L microprocessor ICs production. Potentiostatic regime has been used for anodization of n^+-type regions. Oxidation has been performed by the above-mentioned manner. The obtained structures have exhibited low elastic stresses and low warpage in comparison with those obtained by Isoplanar technology [27]. Devices with IPOS isolation have been subjected to the prolonged climatic testing and withstood the tests with much success. Moreover, it has been possible to form OPS layers integrated with PS gettering layers in the n^+-substrate. This has permitted improving electrical characteristics of bipolar transistors and increase the yield of devices [28].

4. SOI Structures Based on OPS

The method of fabricating SOI structures has been based on the preferential anodization of n^+-layer within the $n^-/n^+/n^-$ structure. Such high selective anodization has been possible because substantially higher voltage has been required to transform lightly doped n^--silicon into PS in comparison with that for heavily doped n^+-layers. So, at low forming voltage anodization process stops as soon as whole n^+-layer has been converted into PS.

We developed this technology for Integral Corporation in 1986–1987. The main steps of the process are shown in Fig. 3. Standard n-type Si (1 0 0) wafers have been used as initial substrates. N^+-layers have been formed by Sb ion implantation into the both front and backside of the substrates followed by annealing at 1220°C. Then, a 0.6 m thick epitaxial layer has been grown on the front of the wafers by chemical vapor deposition at 975°C from dichlorsilane ambient. An α-Si/Si_3N_4 film has been deposited upon the epitaxial layer as a mask layer. Projection photolithography using reactive ion etching of both the mask and the epitaxial layer has been used to define three-dimensional pattern of islands wherein device components should be formed. The anodic treatment of the structure in HF-containing electrolyte has selectively converted n^+-layer into PS underneath silicon islands to be isolated. Enhanced oxidation of PS in comparison with bulk Si has been utilized to oxidize the porous layer within the sandwich structure. Once oxidation of the PS layer has been performed, the Si islands isolated from

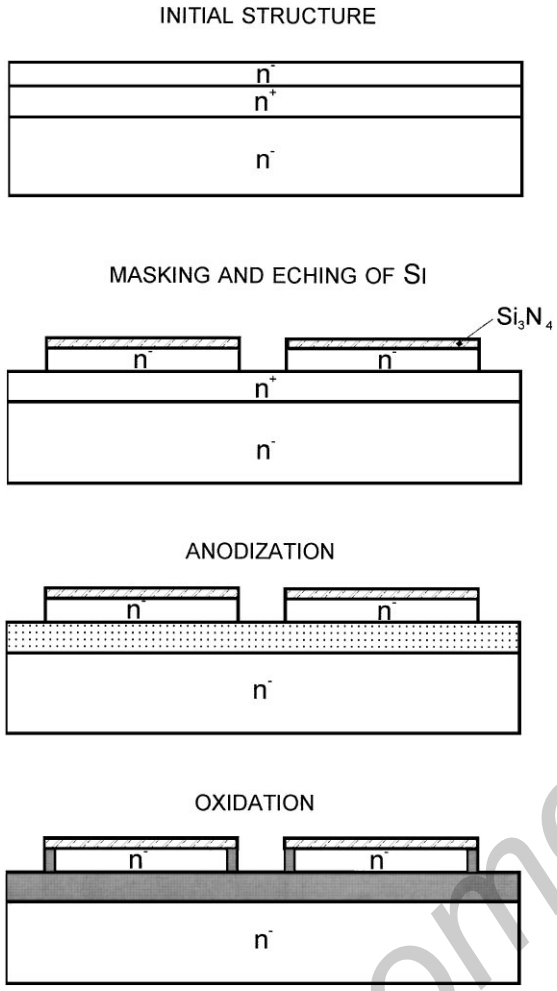

Figure 3. The main steps of OPS-based SOI fabrication.

substrate with the OPS layer have been ready for device fabrication.

OPS uniformity underneath the silicon islands in the lateral direction has been the central problem in the SOI development we have run up against. To overcome it, we have concentrated on both optimizing the process of n^+-layer selective anodization and optimizing the thermal oxidation of PS.

The investigation on selective anodization of the n^+-layer within the sandwich $n^-/n^+/n^-$-structure has provided insight into the kinetic and specific features of the process. It has been found that galvanostatic anodizating regime has been unsuitable for layers with concentration gradient of dopant, as in n^+-buried layer, especially for structures with islands of different size. Potentiostatic regime has been best suited to selective anodization of the implanted n^+-layer within the sandwich $n^-/n^+/n^-$-structure. To obtain SOI structures with low defect level and low warpage, uniform PS layer with ∼56% porosity has been provided by HF solution in isopropanol. Optimal regimes of formation of PS layers with desired porosity have been determined experimentally. The PS layers have been oxidized under high pressure (10 atm) at the temperature of 950°C in dry oxygen. Once oxidized, OPS have been annealed at the temperature of 1200°C in nitrogen to densify OPS. The characteristics of OPS layers have been as follows: resistivity of $(1–4) \cdot 10^{16}$ Ω·cm; the dielectric constant of 3.66–4.2; charge of $7 \cdot 10^{10}$–$3 \cdot 10^{11}$ cm^{-2} [13, 16, 22].

We have succeeded in the conversion into the PS of the n^+-buried layer with minimum thickness of 0.5 μm. With lower thickness PS layer has been found to be not uniform. Maximum thickness of the isolating OPS layer has been within the range of 3–5 μm and has been limited by allowed warpage of the structures (bending deflection at most 20 μm for wafers with diameter of 100 mm). Minimum thickness of isolated Si islands of 0.2 μm have imposed by the width of the transition zone between the n^+-buried and the n^--epitaxial layers.

The 1.2 μm CMOS test matrix has been designed to investigate the SOI structures. The following parameters have been estimated using the matrix. The breakdown voltage between Si islands and the substrate has been 250–450 V depending on the OPS layer thickness. The leakage current density has not exceeded 100 nA/cm^2 at voltage of 10–15 V. The specific leakage currents of p-n junctions in the Si islands have been less than 100 nA/cm^2. The threshold voltage has been adjusted in the value between 0.8 and 1.5 V by variation of boron and phosphorous implantation doses [13, 16, 17, 22].

The 23-stage ring oscillators have been fabricated and packaged to estimate the stage delay in SOI/CMOS gates under various bias voltage (3–5.5 V), temperature (77–400 K), and gamma irradiation. The minimum stage delay has been 200 psec at bias voltage of 5 V. SOI/CMOS ring oscillators have had 40% higher speed in comparison with the same bulk CMOS devices, and continued stable operating under bias voltage 3–5.5 V, gamma irradiation up to 10 Mrad(Si), and environment temperature 77–400 K [16].

To demonstrate potentialities of the SOI technology, high-speed logic ICs of 74AC series has been developed. These ICs in SOI structures and in bulk Si have been manufactured at the same time, in the

same conditions of manufacturing production. Switching times of ICs manufactured in SOI structures have been less than these of ICs manufactured in bulk Si by a factor 1.8–2.

5. Waveguides Based on Oxidized Porous Silicon

Our experience in the OPS technology has been used for development of channel integrated optical WGs. Channel WG has been a guide with a limited width embedded or buried more or less deeply inside of the substrate. In order to provide confinement and propagation of light within the WG, the guiding region (core) has to have a higher refractive index than the surrounding cladding regions. In the channel WG demonstrated in Fig. 4 the core part has consisted of the dense OPS layer with refractive index of 1.458. The surrounding cladding regions have been porous OPS layers with low porosity and refractive index of 1.446.

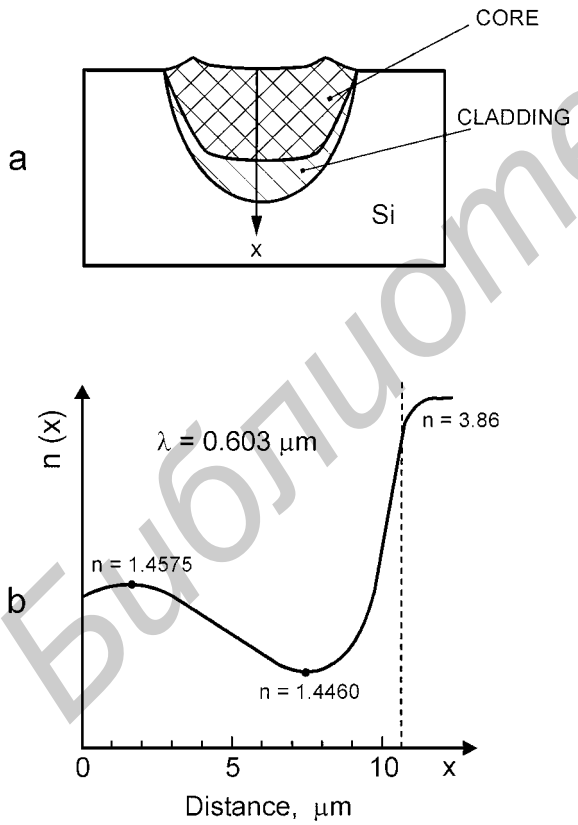

Figure 4. Cross-section of the OPS-based waveguide (a) and the radial distribution of refractive index over the waveguide cross-section (b).

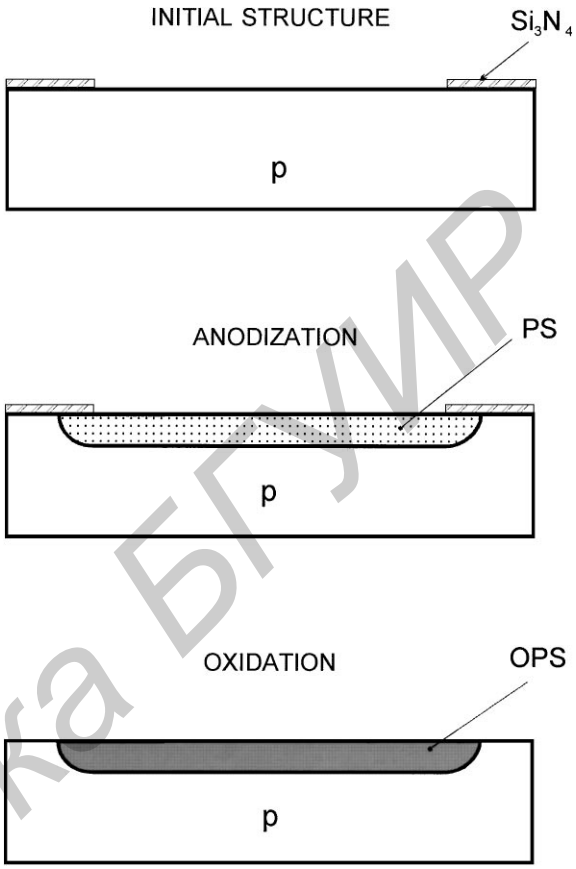

Figure 5. The main steps of the OPS-based waveguide fabrication.

Such construction of WG can be provided by a variation of anodization regimes when PS has been formed. Two types of optical WGs have been feasible: multimode and monomode. The guiding core of the multimode WG has been large (10 μm and more) in comparison with the guiding core of the monomode WG (less than 5 μm). OPS as wavegiding material have special features to suit the following requirements: (i) optical characteristics along the WG length should be uniform; (ii) core and cladding regions should have essentially different refractive indexes; (iii) interfaces core-cladding regions, OPS-silicon substrate, and outer surface of OPS should exhibit minimum roughness. Moreover, OPS based WG can be used successfully provided that there have been low optical losses and a broad transmission spectrum.

The technological process of a WG fabrication has been similar to the p^+-IPOS process and has consisted of three main steps as shown in Fig. 5: (i) anodization of p-type Si through the openings in the Si_3N_4 mask

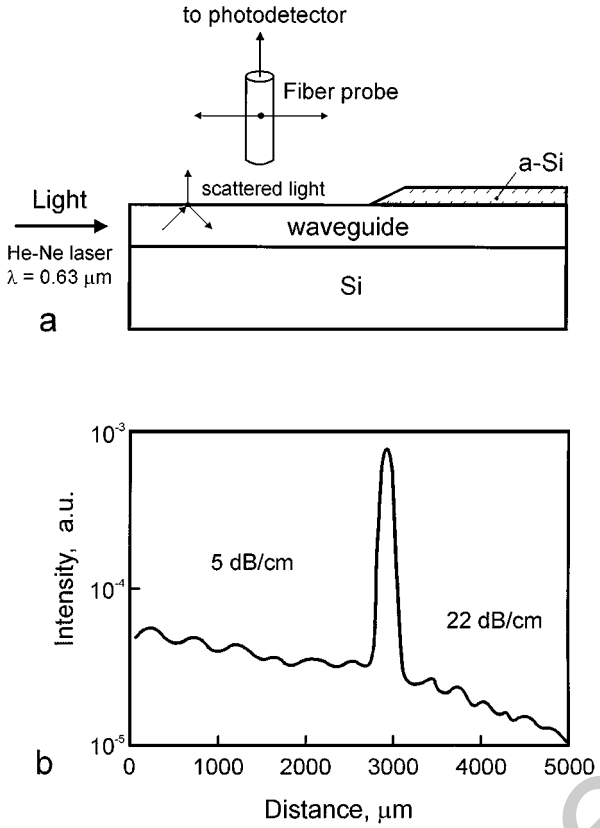

Figure 6. Scheme of the out-of-plane scattering losses measurement (a) and plot of scattered light intensity vs. distance along the waveguide (b).

to form PS; (ii) thermal oxidation of PS; (iii) high-temperature densification of OPS. The "soft" regimes of the thermal oxidation and annealing together with proper choice of PS parameters have provided a low level of elastic stress, absence of cracks and dislocation glide lines [18–20]. The WGs have had a length of 1.5–3.0 cm and a thickness of 5–15 μm. Buried multimode channel WG based on OPS has been well adapted for production of multimode devices like beam splitters.

Referring to Fig. 6, scattering losses from the surface of the OPS have been determined to be about 5 dB/cm on almost 3 mm waveguiding length, at $\lambda = 632.8$ nm exciting wavelength. This result has been quite promising for optoelectronic applications [20, 29]. The strong attenuation of optical signal in the part of the waveguide covered with amorphous Si has been observed to provide a good background for the development of a-Si : H photodetector integrated with OPS-based waveguide.

Rare-earth element doping and thermal treatment can drastically change optical properties of OPS. In particular, OPS doped with erbium has been shown [30] to exhibit sharp luminescence at 1.54 μm. Such OPS : Er waveguide structures have been promising for integrated optical filters, amplifiers/modulators, and other optoelectronic devices.

6. Conclusions

In conclusion, we have presented the brief review of the steps forward in OPS applications for dielectric isolation of components of bipolar and CMOS ICs. While these techniques have found limited current commercial use, experience gained from 20-years OPS research have been applicable to the fabrication of optoelectronic OPS-based devices. Specifically, OPS-based integrated optical WGs have been demonstrated. A variety of derived devices (splitters, couplers, modulators, etc.) can be constructed within the WGs based on OPS.

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