Reliability Assessment of the Nano-dimensional Dielectrics of the Submicron Microcircuits

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In production of the modern submicron integrated circuits (ICs) the enhanced requirements are posed to the gate dielectric, whose thickness constitutes less than 5 nm. The thin gate dielectric in many respects determines the Ics' reliability. Presence of the defects substantially affects the dielectric's reliability, and the efficient method for reliability assessment of the thin dielectrics, making it possible to reject the potentially unreliable wafers in the process of the Ics production technological cycle is of utter relevance. The novelty of this work is that the suggested technique is intended for the express reliabiity assessment of the gate dielectric 1 – 50 nm thick at the stage of the integrated circuits' chips fabrication. This makes it possible to enhance controllability of the technological processes and to ensure arrival for assembly of the potentially reliable IC chips.

The proposed method is based on the express determination of the error-free running time of the gate dielectric of the MIS-integrated circuits at the expense of the reproductible, automated determination of acceleration ratios of the dielectric degradation when tested. The test MIS-structure is subjected to the passing of the electric charge through the gate dielectric until its breakdown. Meanwhile through the structure the ramp-increasing current (from 1 nA to 100 mA) is passed with the constant duration of all steps. For the sake of ensuring the required test precision 50 steps were preset for the each order of the current value variation. On passing each current step they measure up the leakage current value of the MIS-structure with the voltage, equal to the operating voltage of the integrated circuit. The test is terminated after the structure's breakdown. In the process of trials of the test structure, when passing the i-th step of the charge Q_i there occurs the *i*-th stage of the dielectric's accelerated degradation during the time t_{pulse}. The given stage of the accelerated degradation can be substituted for the equivalent degradation under the operational conditions. For this the time is required, exceeding duration of the i-th current step the number of times, equal to the ratio of the charge value Q_i to the average leakage current value through dielectric, measured under the IC operational conditions. The error-free running time value is determined as a total of the dielectric degradation times applicable to the operational conditions, determined for all current steps until the moment of the dielectric's breakdown.

Thus, the proposed method of determining the error-free running time of the gate dielectric of the MIS-integrated circuits ensures the control express-time at the expense of the ramp-increasing current and the reproductible, automated determination of the acceleration ratios of the dielectric's degradation during tests. The method is effective for the efficient detection of the potentially unreliable products at the IC chips fabrication stage and for maintaining the technological process of the ICs production at the required level. This makes it possible to ensure arrival for assembly of the potentially reliable IC chips and is a certain reliability guarantee of the packaged integrated circuits. A sunstantial advantage of the proposed method is a possibility of the direct reliability assessment of the gate dielectric of the integrated circuits within the operating temperature range from minus 65 ^{0}C to plus 125 ^{0}C.