Similar patterns are observed for neutrons and protons fluxes. So for a neutrons flux with an energy of E_N = 1,5 MeV, the fluence value, at which the dependence of the width of leading edge ceases to be linear, is $F_N = 8 \cdot 10^{14}$ cm^{-2}. For the protons flux with an energy of E_P = 2 MeV, the fluence value is $F_P = 2 \cdot 10^{11}$ cm^{-2}.

IV. CONCLUSIONS

The results of modeling electrical characteristics of the device structure p-channel JFET showed acceptable agreement with the experimental data in the temperature range from 383 K to 223 K. The pinch-off voltage at 303 K is 1,31 V (measured at 1,29 V), the drain current is 3,9 mA (3,4 mA), for temperatures 383 K and 223 K the value of these characteristics is 1,49 V (1,43 V) and 2,85 mA (2,7 mA), 1,17 V (1,15 V) and 4,58 mA (2,68 mA), respectively.

Through a series of computer experiments, the assumption [6] of the equality of degradation effect introduced by electrons fluxes, neutrons and protons with a fluences F_E with an energy of E_E = 4 MeV, $F_N = 0{,}302 \cdot F_E$ with an energy of EN = 1,5 MeV or a fluence $F_P = 1.1 \cdot 10^{-4} \cdot$FE with an energy E_P = 2 MeV was checked.

Dependence of the degradation effect of influence particle flux on temperature is shown. For the considered device structure of the p-channel JFET, it has been established that, with decreasing temperature, the effect of the influence of electrons flux increases.

The results of the effect of particle flux on the width of leading and trailing edges when switching the device structure of p-channel JFET were given. The values of the fluences of electrons, neutrons and protons for which the change in the width of leading edge ceases to be linear ($F_E = 2 \cdot 10^{15}$ cm^{-2}, $F_N = 8 \cdot 10^{14}$ cm^{-2}, $F_P = 2 \cdot 10^{11}$ cm^{-2}) are determined.

ACKNOWLEGMENTS

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OPTIMIZATION OF STRUCTURAL AND TECHNOLOGICAL PARAMETERS OF JUNCTION FIELD-EFFECT TRANSISTOR WITH INCREASED RADIATION HARDNESS

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I. INTRODUCTION

The solution of process tasks [1] in creating a microelectronic radiation-hardened hardware components and the development of «special» circuity engineering [2] in recent years is given increased attention. Synthesis of high-quality analog ICs, that are low-sensitivity to the effects of penetrating radiation, is advisable to perform on bipolar transistors (BT) and junction field-effect transistors (JFET) with a large boundary frequency [3, 4]. The results of the investigation radiation hardness of ABMK version 1_2, (JSC

"INTEGRAL"), which show that p-JFETs has the highest radiation hardness, and the smallest – the side transistors of p-n-p type are given in [1]. The radiation hardness of JFETs is explained by the fact that their functioning is caused by the motion of the majority carriers far from the surface and the radiative change in the state of the surface does not have a significant effect on the parameters. The JFET device structures are more susceptible to discomposition effects, which lead to the formation of radiation defects in the crystal [5]. The increased interest is shown to the possibility of creating a complementary pair of JFET within the framework of a single technology process, which has an increased radiation hardness.

II. STRUCTURE

JFETs belong to the category of normally open field-effect transistors, in which the conducting channel and, consequently, the current in the channel close to the maximum, exist at zero gate voltage (VG = 0 V). JFETs are also called depletion devices, since when a voltage is applied to the gate, the channel is depleted by carriers of electric current and the current in the channel decreases.

The active region of the device structure of n-JFET under study is shown in Fig. 1. Substrate of the hole-type conductivity, doped boron with a concentration of 1,35·1015 cm-3, crystallographic orientation (111). For this device structure, the nominal values of the pinch-off voltage VGoff and drain current ID are respectively – 0,9945 V and 0,0129 A.

In the modeling of the manufacturing technique of n-JFET, 11 stages are conditionally allocated: assignment of the substrate and computation grid, sequential formation of regions of the n-well, p+-buried layer, the conduct of epitaxy, the formation of oxide isolation, the p-well regions, n-collector, n-base, opening of areas for contacts (together with oxidation of the substrate surface), formation of regions p+-emitter, n+-emitter, metallization.

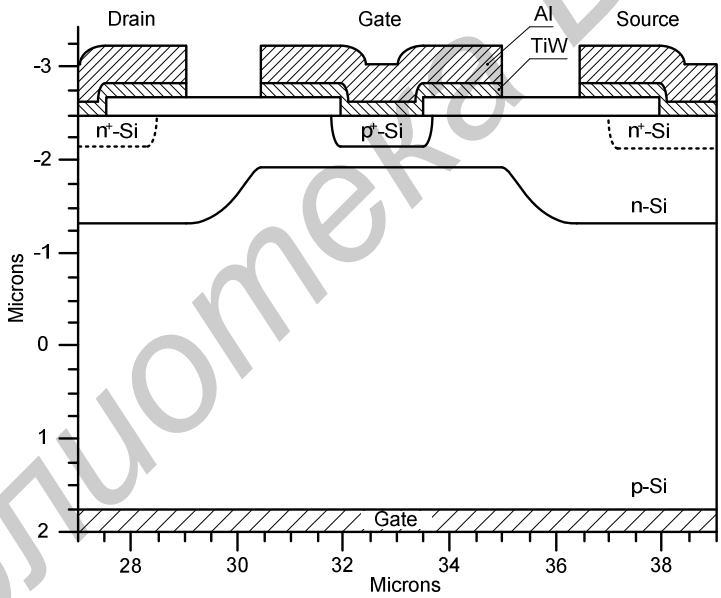

Figure 1 – Active area of the device structure of n-JFET

III. RESULTS

The influence a deviation of the parameters of processing procedures on the electrical performance of the device structure n-JFET, exposed to a neutrons flux with an energy EN = 1,5 MeV has been modeled.

For the selected stages of the manufacturing technique, 33 parameters are defined (the parameter designation in the simulation is indicated in brackets): boron concentration (X01) in the initial substrate, dose (X02) and energy (X03) of antimony ions during implantation #1, time (X04) and temperature (X05) annealing after implantation #1, dose (X06) and energy (X07) of boron during implantation #2, time (X08) and temperature (X09) of annealing after implantation #2, thickness (X10) of epitaxial layer and concentration (X11) phosphorus in it, time (X12) and temperature (X13) of the thermal oxidation of silicon, dose (X14) and energy (X15) of boron ions during implantation #3, time (X16) and temperature (X17) of annealing after implantation #3, dose (X18) and energy (X19) of phosphorus ions during implantation #4, time (X20) and temperature (X21) of annealing after implantation #4, dose (X22) and energy (X23) of phosphorus ions during implantation #5, time (X24) and temperature (X25) of annealing after implantation

#5, dose (X26) and energy (X27) of boron ions during implantation #6, time (X28) and temperature (X29) of annealing after implantation #6, dose (X30) and energy (X31) of phosphorus ions during implantation #7, time (X32) and temperature (X33) of annealing after implantation #7.

Analysis of the results of modeling the dependence of the drain current ID n-JFET on the drain voltage VD with the gate voltage VG = 0 V and exposure to neutrons fluence FN = $2 \cdot 10^{14}$ cm^{-2} with an energy EN = 1,5 MeV for various modes of processing procedures showed, that the greatest influence temperatures on the radiation hardness to the neutrons flux at which the processing procedures of thermal oxidation (X13) and annealing after implantation #3 (X17), #5 (X25), #6 (X29) and #7 (X33) are carried out. The deviation of the drain current dID under the influence of the fluence of neutrons FN = 2·1014 cm-2 with an energy EN = 1,5 MeV from the value without influence during changing these parameters is shown in Fig. 2. The change in the annealing temperature (X09) after implantation #2, energy (X23) of phosphorus ions during implantation #5, dose (X26) and energy (X27) of boron ions during implantation #6, time of annealing (X32) after implantation #7 has a smaller response t to the radiation hardness of the device structure of n-JFET (maximum value for parameter X09 t = 0,027% deviation of drain current dID by one percent of parameter change, and minimum for parameter X33 t = 0,062%). The remaining parameters have practically no effect on the deviation of drain current dID under the influence of the fluence of neutrons FN = 2·1014 cm-2 with energy EN = 1,5 MeV.

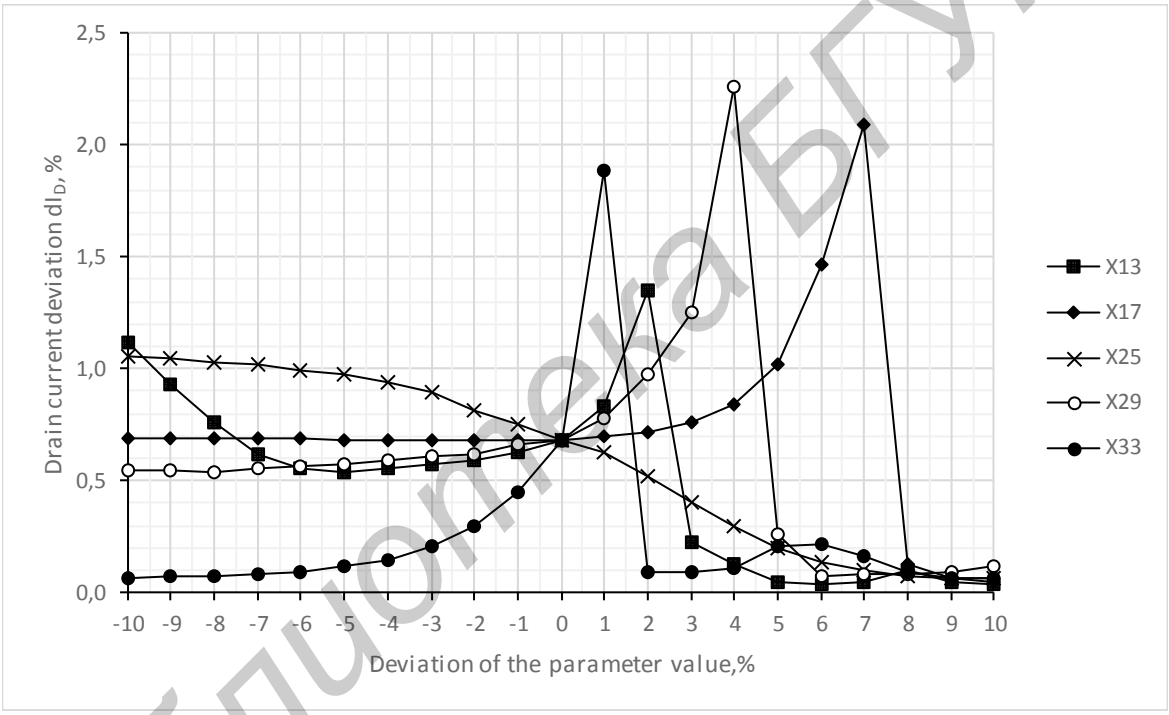

Figure 2 – Dependence of the deviation of drain current dID from the nominal value when exposed to fluence of neutrons FN = $2 \cdot 10^{14}$ cm^{-2} with an energy EN = 1,5 MeV when change the parameters of the manufacturing technique of n-JFET

Changing the modes of processing procedures also affects other electrical performance of the device structure n-JFET. Dependence of drain current dID on the change of parameters X13, X17, X25, X29, X33 is showm on the Fig.3. It can be seen from the simulation results, that all parameters have a significant effect on the drain current ID (when the values of the parameters X25 and X33 change from 0,9·Pnom to 1,1·Pnom, the drain current ID increases and decreases by three orders of magnitude, respectively). Dependence of pinch-off voltage VGoff on the change of parameters X13, X17, X25, X29, X33 is shown on the Fig.4. It can be seen from the simulation results, that all parameters have a significant effect on the pinch-off voltage VGoff (when the values of the parameters change from 0,9·Pnom to 1,1·Pnom, the pinch-off voltage VGoff increases for parameter X25 and decreases for parameters X33 and X33 more than four times).

Thus, when optimizing the design features and modes processing procedures for increasing the radiation hardness of the device structure n-JFET, the use of parameters X13, X17, X25, X29, X33 is difficult if you need to save the value pinch-off voltage (compliance with the complementarity condition).

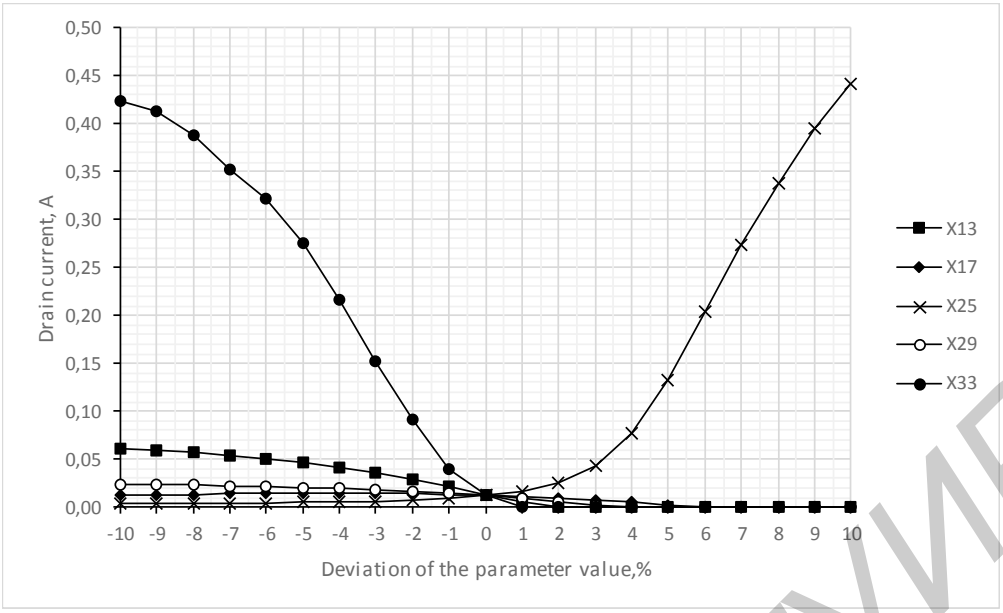

Figure 3 – Dependence of drain current ID on the change of the parameters of manufacturing technique n-JFET

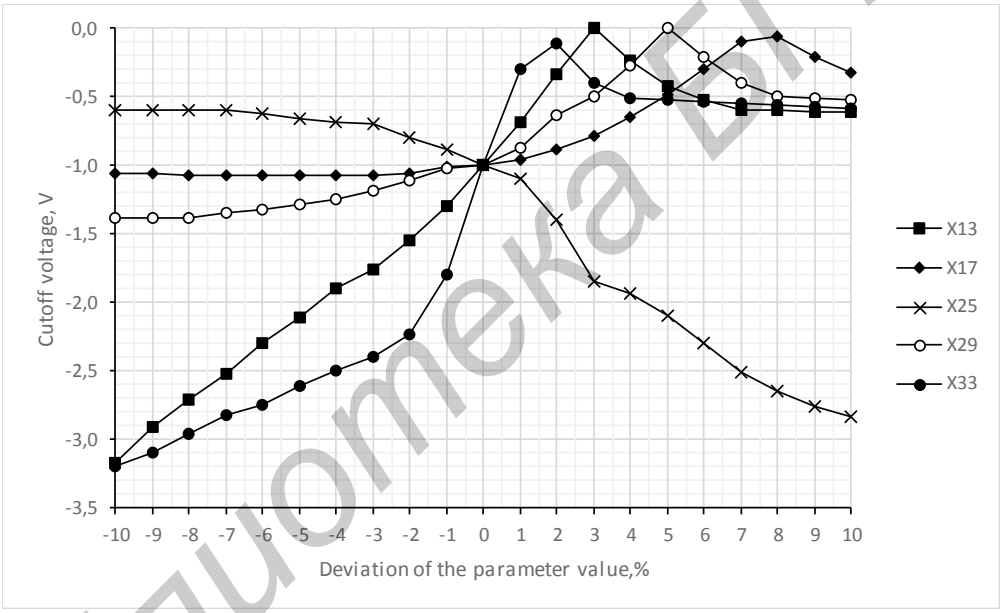

Figure 4 – Dependence of pinch-off voltage value VGoff
on the change of the parameters of manufacturing technique n-JFET

As a result of optimization calculations using the modified Levenberg-Marquardt algorithm for constructing the response surface describing the dependence between the input parameters and the output characteristic in the iterative process, the values of the modes processing procedures were obtained that ensure a deviation of the drain current value by no more than 0,5 % when exposed to the neutrons fluence FN = $2 \cdot 10^{14}$ cm^{-2} with an energy EN = 1,5 MeV. For the optimized device structure, nominal values of the pinch-off voltage VGoff and drain current ID are respectively -1,041 V and 0,0136 A. Dependence of the deviation of drain current dID for the initial and optimized structure under the influence of different neutrons fluences is shown on Figure 5.

It can be seen from the simulation results that for an optimized device structure, the influence of neutrons flux with an energy EN = 1,5 MeV is reduce by 1,45 times (deviation of the drain current under the action of the fluence of neutrons F = $1 \cdot 10^{6}$ cm^{-2} is equal to dID = 0,343% and dID = 0,236%, when the fluence of neutrons F = $6 \cdot 10^{6}$ cm^{-2} is equal to dID = 2,047% and dID = 1,412% for the basic and optimized device structure of the n-JFET, respectively).

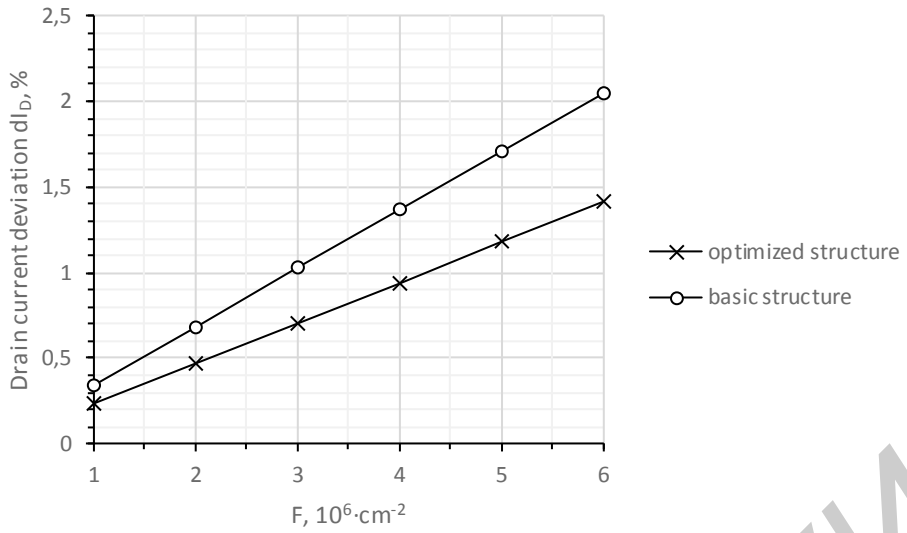

Figure 5 – Dependence of the deviation of drain current dID under the influence of different neutrons fluences F with an energy EN = 1,5 MeV for the initial and optimized device structure n-JFET

IV. CONCLUSIONS

Structural and technological parameters that have the greatest influence on the deviation of the drain current value ID at the action of the fluence of neutrons FN = $2 \cdot 10^{14}$ cm^{-2} with an energy EN = 1,5 MeV are determined. It is established that the use for the optimization of the radiation hardness of electrical performance for the neutrons flux of device structure n-JFET, parameters modes of processing procedures of the thermal oxidation (parameter X13) and annealing after implantation in the formation of areas p-well (X17), n-base (X25), p+ -emitter (X29), n+ -emitter (X33) leads to a spread in the pinch-off voltage values VGoff and the drain current ID up to the inoperability of the device. So, when the parameters value is changed, the pinch-off voltage VGoff increases for the parameter X25 (VGoff = -0,593 V at 0,9·Pnom to VGoff = -2,834 V at 1,1·Pnom) and decreases for parameters X13 (VGoff = -3,166 V at 0,9·Pnom to VGoff ≈ 0,0 V at 1,03·Pnom) and X33 (from the value of VGoff = -3,194 V at 0,9·Pnom to VGoff ≈ -0,001 V at 1,05·Pnom) more than four times.

As a result of optimization calculations using the modified Markar-Levenberg algorithm, the values of the modes of processing procedures were obtained that ensure the deviation of drain current ID value by no more than 0,5% when fluence of neutrons FN = $2 \cdot 10^{14}$ cm^{-2} with an energy EN = 1,5 MeV. For the optimized device structure, the nominal values of the pinch-off voltage and drain current density are respectively equal -1,041 V and 0,0136 A, the effect of the neutrons flux with an energy EN = 1,5 MeV is reduce by 1,45 times in comparison with the basic structure.

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PARALLEL COMPUTING ENVIRONMENT FOR DIGITAL DEVICES SIMULATION AND VLSI TOPOLOGY VERIFICATION

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INTRODUCTION

During several decades semiconductor (digital) electronics is developed exponentially according to Moore's Law. By now the number of transistors on chip for wide application ICs has exceeded 2.5 billion, and has reached 8 billion in the segment of graphics processors. On the one hand this allows to place a projected device including interface components on one chip entirely, which significantly increases the manufacturability and reliability of the device. On the other hand the complexity of the designed devices increases greatly. In this connection several problems appear, among which the following ones can be noted increasing time of design, verification and reliability control of digital ICs and the equipment based on them. Design of the digital electronic devices is a cyclical process. Design cycle includes a series of consecutive steps with different computational complexity, such as description compilation and synthesis, circuit simulation, tracing into the crystal, simulation at the crystal level. These steps are usually performed automatically under the control of a project developer with the use of computational tools and specialized programs included in CAD. Implementation of a series of steps using CAD of widely known companies, such as Actel, Xilinx and Mentor Graphics, even for small devices with hundreds of thousands of equivalent gates can take up to several hours of computer time even on a hi-end class multi-core personal computer (PC).

With an increasing project size the number of development-testing cycles increases, which leads to more than linear growth of development time as a whole. As a result, design and debugging of digital devices can take from several months to one year despite the high performance of desktop computers, while in today's market conditions success of a product can completely depend on how a manufacturer (supplier) outstrips the competitor.

The stage of project testing (verification) is the most critical and time consuming stage in the whole process and it can take up to 90% of the total development time. The number of verification tests for a large project can reach thousands and all of them are performed consecutively if typical CAD software that runs on a standard PC is used for development.

II. PARALLELIZATION OF TESTS FOR LIBERO CAD AND XILINX CAD

Both in Actel Libero CAD and in Xilinx ISE CAD Mentor Graphics ModelSim program can be used as a software tool for devices simulation. The main operating mode of ModelSim is graphical. Two methods are used for ModelSim configuration: modelsim.ini and do file. Both of these files are generated in both CAD dynamically for each simulation run. Use of the files as a data exchange mechanism and for parameters transmission allows to carry out the simulation not only in the graphical, but also in the batch mode, which allows to perform the device simulation parallel using several computational nodes by placing a different part of a task on each node.

Fig. 1 shows the scheme of user interaction with ModelSim simulator in the case of classical, as provided for by a typical design technical process, and parallel implementation.

In the case of classical implementation the user carries out the instruction to start the simulation with CAD. The CAD prepares data based on project content for simulation. Data for simulation are the file that contains a device model and the file that contains simulation parameters. Also in addition to these two files, additional files with components that can be used from the model file, as well as files with a description of time delay of a device can be transmitted to the simulator. The prepared data in do file form are transmitted