THE DIFFERENCES AMONG ESD PROTECTION METHODS

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Abstract – This paper explains and describes performance and advantages of HBM test standards for prediction influence of ESD stress impact. With this key information, you can design more effective ESD control programs.

Electro-Static Discharge (ESD) is one of serious problems for modern integrated circuits (IC) and other

semiconductor devices. Thinner gate oxides, complex chips with multiple power supplies, mixed signal blocks and faster circuit operations all these contribute to increased ESD-sensitivity of advanced semiconductor products [1,2]. So, to predict ESD appearance and its influence we need to carry out a simulation of an actual ESD impulse. Usually, ESD testing models include such standards as Human Body Model (HBM), Machine Model (MM), and Charged Device Model (CDM).

The HBM model is intended to simulate a person becoming charged and discharged from a finger to ground through the circuit or device under test (DUT). The basic HBM model [3] is shown in Figure 1. A 100 pF capacitor is charged by a high voltage power supply, and a relay initiates the HBM stress pulse through a 1500Ω resistor to the DUT.

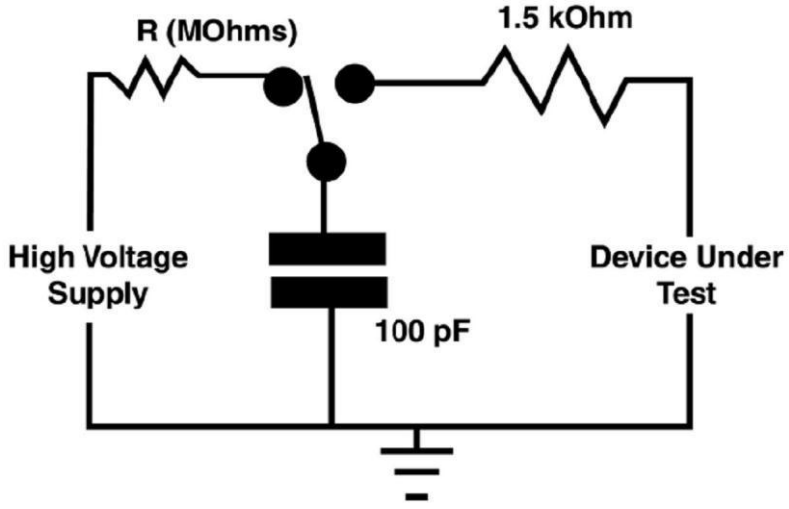

Figure1. Typical HBM model circuit.

Processes such as packaging, final testing, shipment, placement on the circuit board, and the soldering process should be controlled to limit the level of ESD stress to which the device is exposed. In the manufacturing environment ICs can withstand only 2 kV HBM, some can withstand 8 kV, while others – particularly newer parts in very small geometry devices – only 500 V or less [4]. But while HBM is usually sufficient for the controlled ESD environment of the factory floor – it is completely inadequate for system level testing. In the end user environment the levels of Electro-Static voltages and currents can be much greater. For this reason, there are different testing standards for ESD system level testing. One of them is IEC 61000-4-2 [5].

The IEC 61000-4-2 standard is a system level test that replicates a charged person discharging to a system in a system end user environment.

The implementation of HBM ESD testing standards for manufacturing is much differs from the usage of system level testing standards. The traditional HBM test standard is intended to ensure that integrated circuits withstand the manufacturing process. Usually the system level testing standard ensures that finished products withstand normal operation environment. In this case, the user of the product should not think about lowering ESD stress. The IEC 61000-4-2 is a more stringent standard. It allows identifying and correcting ESD vulnerability of electronic products under real-world ESD stress conditions.

It is important for system designers to know differences between various ESD test standards. The value range used for protection ICs in the manufacturing environment such as HBM and CDM differs from similar values of system level ESD test, e.g. such as the IEC 61000-4-2. Misapplying of these standards can result in design flaws and/or product returns.

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