High performance multiplier-less pipelined FPGA architecture for 2-D non-separable quaternionic filter banks

Eugene V. Rybenkov [1],

Nick A. Petrovsky [2]

1, 2 Computer Engineering Department, Belarusian State University of Informatics and Radioelectronics, Minsk, Belarus

Keywords: quaternionic paraunitary filter banks; two-dimensional; non-separable transform.

Abstract: This paper presents a systematic design of the 2-D non-separable quaternionic paraunitary filter banks $(Q -$PUFB) based on the integer-to-integer invertible quaternionic multiplier applied to image processing. In order to achieve higher transform coding gains in multidimensional domain with relatively low-complexity implementation, orthogonal transform 8-channel $Q -$PUFB factorize into two-dimensional non-separable structures called ”64in-64out” (2D NS $Q -$PUFB). The given structures can be mapped directly to parallel-pipelined processor architecture with minimal latency time $4 (N +1)$ quaternion multiplication operations, where N is transform order of $Q -$PUFB. The latency of parallel-pipelined processing does not depend on the size of the original image. Experimental design results on resource utilization and total throughput are obtained using a Xilinx

Ultrascale + FPGA Series. System prototype total throughput variates from 13.8 up to 55 million pixels per second and depends on fixed point constraints.

This article publisjed in: Rybenkov, E. V. High performance multiplier-less pipelined FPGA architecture for 2-D non-separable quaternionic filter banks // E. V. Rybenkov, N. A. Petrovsky // Signal Processing: Algorithms, Architectures, Arrangements, and Applications (SPA'2020): Proc. 24st Int. Conf., Poznan, Poland, September 23-25. – 2020 / Poznan University of Technology. – Poznan, 2020. – P. 42-47. – DOI: 10.23919/SPA50552.2020.9241273.

Internet-link to this article:

https://ieeexplore.ieee.org/abstract/document/9241273 .