THE BASICS OF MEMORY FAULT DETECTION WITH MARCH TESTS

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Annotation. The article focuses on detecting memory matrix faults. The trends in the evolution of storage devices are considered and the generalized memory model is provided. The classification of single-cell fault models and the dominant testing method are given. The article shows the advantages and disadvantages of march tests.

Keywords. Memory system testing, memory fault models, single-cell faults, march tests.

The memory system has the largest part in terms of the number of chips and their total cost in modern computing systems. The evolution of technologies leads to an exponential reduction in the size and increase in the capacity of storage devices. The problem of testing storage devices in modern computing systems, such as embedded systems, systems-on-a-chip and nets-on-a-chip, is a very relevant problem. Along with the increase in storage capacity, the requirements for their reliability increase, so the role of testing is very important [1-4].

The functional model of a memory chip consists of many blocks. The generalized memory model is shown in Figure 1 [5]. Block A is used to set the address of the cell for the read or write operation. The cells are stored in the matrix, therefore, to determine their location, the address contains data about the row and column, which are decrypted in blocks B and C. The array of storage elements is marked with the letter D, the read/write logic occurs in blocks E, F, G.



Figure 1. Functional model of a memory chip

Failures of the electronic frame and the matrix of storage elements are the reasons for the incorrect state of the memory. The electronic frame includes an address decoder and read/write logic [6]. Testing

the memory array is a major focus. Despite its simple organization, there is a huge variety of possible faults, and the detection and classification of some of them is a difficult task.

Faulty states of storage devices are described by mathematical models. A fault model is an abstraction of an error caused by a specific physical defect. The purpose of the fault model is to simplify the testing procedure and reduce its cost.

Memory faults can be differently divided into subclasses. The most common classification is based on the number of cells. Memory faults can involve one, two, or more cells. Single-cell faults include stuckat-fault and transition faults [6]. The stuck-at-fault (SAF) is one in which the logic value of a cell or line is always zero (SA0) or always one (SA1). The cell cannot change its state. The transition fault (TF) is a special case of the SAF, in which a cell cannot make the transition from zero to one or from one to zero.

In order to test the memory completely, you need to write and read all possible combinations of zeros and ones in the memory array. The time for such testing is proportional to the value of 2N, where N is the memory capacity in bits. The current memory size does not allow performing the test with such complexity. In the early 1980s, after the introduction of fault models, march tests became the dominant testing method. Two advantages of march memory tests are high fault coverage and acceptable test time, which depends linearly on the memory size [7]. These tests are characterized by a simple hardware implementation, which is very important for built-in self-testing tools (built-in self-test – BIST) [6].

The march test consists of a finite sequence of march elements, which is written in curly brackets. A march element is a finite sequence of read and/or write operations that is applied to each memory cell. A set of possible operations are 'r0' – read operation with the expected value of zero, 'r1' – read operation with the expected value of zero, 'w1' – write operation of one. Each march element has an indication of the order of the address sequence: ascending address order (1) or descending address order (1). The symbol '1' indicates that the address order is not relevant [6].

MATS test is the simplest example of classic march tests. The test has the following sequence: $\{ \hat{\Pi} \Downarrow (w0); \hat{\Pi}(r0,w1); \Downarrow (r1) \}$. The test execution time is proportional to the value of 4N, but it completely covers only constant faults. MATS++ test is another example of march tests. Its sequence: $\{ \hat{\Pi} \Downarrow (w0); \hat{\Pi}(r0,w1); \psi(r1,w0,r0) \}$. The complexity of MATS++ is 6N [8]. It detects all single-cell faults, both constant and transient.

March tests successfully detect single-cell and simple two-cell faults. However, as the density of memory cells increases, faults become more complex. Memory fault can involve three or more memory cells. They affect each other by changing each other's content. The process of detecting these faults is very time-consuming.

References:

1. Bushnell, M. L. Essentials of electronic testing for digital, memory and mixed-signal VLSI Circuits / M. L. Bushnell, A. Vishwani. – NY: Kluwer Academic Publishers, 2001. – 690 p.

2. Wang, L. T. VLSI Test Principles and Architectures: Design for Testability / L.T. Wang, C.W. Wu, X. Wen. – San Francisco, CA, USA: Morgan Kaufmann Publishers Inc., - 2006. – 808 p.

3. Yarmolik, V. N. Kontrol' i diagnostika vychislitel'nykh sistem [Monitoring and Diagnostics of Computer Systems]. Minsk, Bestprint, 2019, 387 p. (Russian).

4. Mazumder, P. Parallel Testing for Pattern Sensitive Faults in Semiconductor Random Access Memory / P. Mazumder, J. H. Patel // IEEE Transactions on Computers. – 1986. – Vol. 38, iss. 14. – P. 394-407.

5. Keon-Jik, L. A simple diagnostic method for memory testing / L. Keon-Jik // Proceedings of the 2nd WSEAS International Conference on Electronics, Control and Signal Processing. – Wisconsin, United States, 2003. – №16. – P. 1-6.

6. Yarmolik, S. V., Zankovich, A. P., Ivanyuk, A. A. Marshevye testy dlya samotestirovaniya OZU [RAM Self-Test March Tests]. Minsk, Bestprint, 2009, 271 p. (Russian).

7. Hamdioui, S. Testing Embedded Memories: A Survey / S. Hamdioui // Mathematical and Engineering Methods in Computer Science. MEMICS 2012. Lecture Notes in Computer Science. – Heidelberg, Germany, 2013 – Vol. 7721. – P. 32-42.

8. Zakaria, N. A. Testing Static Single Cell Faults Using Static and Dynamic Data Background / N. A. Zakaria, W. Z. W. Hasan, I. Abdul Halin, R. M. Sidek, X. Wen // IEEE Student Conference on Research and Development. – Cyberjaya, Malaysia, 2011. – P. 1-6.