Robust performance and stability of In2O3 thin-film transistors with atomic-layer-deposited channels

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Abstract

Atomic-layer-deposition (ALD) In₂O₃ thinfilm transistors (TFTs) were fabricated under a maximum processing temperature of 200 °C. In order to reduce the concentration of oxygen vacancies in the In2O3 channel, O2 plasma treatment was carried out on the TFTs by plasmaenhanced chemical vapor deposited (PECVD). The In₂O₃ TFT treated at 200 °C for 240s exhibited good performance such as a field-effect mobility of 11cm²/V·s, a threshold voltage (V_{th}) of 0.9 V, a subthreshold swing of 0.38 V/dec. and an on/off current ratio of 107. In addition, the device exhibits a small negative threshold voltage shift (ΔV_{th}) during negative gate bias stress. However, it showed a more pronounced ΔV_{th} under positive bias stress with a characteristic turnaround behavior from a positive ΔV_{th} to a negative ΔV_{th} . The positive ΔV_{th} is attributed to the charge trapping effect, and the abnormal negative ΔV_{th} should due to the hydrogen incorporated into the film.

Results

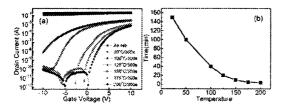


Figure 1a: Transfer characteristics of In₂O₃ TFTs annealed at 300°C for different time in air Figure 1b: Dependence of the treatment time of the optimized In₂O₃ TFT on treatment

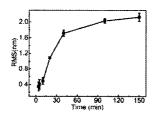


Figure 2: RMS roughness of In2O3 surface measured by AFM as a function of O2 plasma treatment time

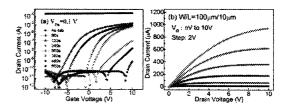


Figure 3a: Transfer characteristics of the In₂O₃ TFT treated by O₂ plasma at 200°C for different times

Figure 3b: Output characteristics of the In₂O₃ TFT treated at 200°C for 240s

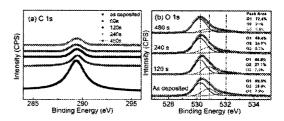


Figure 4: High resolution (a) C 1s and (b) O 1s XPS spectra of the \ln_2O_3 films treated by O_2 plasma for different time, respectively. To remove adventitious surface contaminants, all the samples were etched with in-situ Ar ion bombardment for 3 min before signal collection

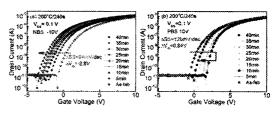


Figure 5: Typical stress time-dependent transfer curves of the ln_2O_3 TFT treated by O_2 plasma at 200°C for 240s, under (a) negative gate bias stress (V_G = -10V) and (b) positive gate bias stress (V_G =10V), respectively