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Metallization of Vias in Silicon Wafers to Produce Three-Dimensional Microstructures

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Abstract—The processes of electrochemical deposition into a matrix of vertical vias of different diameters (500–2000 nm) in Si/SiO_2 substrates with a TiN barrier layer at the bottom of the holes are studied. Morphological studies of the metal in the holes show that the structure of copper clusters is rather uniform and is formed from crystallites of ~30 to 50 nm. Repeatability and stability with a homogeneous structure and with holes filled 100% by Cu determine the prospect of using the $Si/SiO_2/Cu$ system as a basic element for creating three-dimensional micro- and nanostructures, as well as for the 3D assembly of IC crystals.

Keywords: electrochemical deposition, copper, barrier layer, three-dimensional assembly of crystals, metallization, morphological characteristics

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INTRODUCTION

The most serious technical problems in manufacturing modern ICs are related to the formation of metal interconnections. A large number of contact pads of the upper level of metallization when they are connected to the contact pads of IC packages makes this operation expensive which significantly increases the cost of the finished product and reduces the reliability of such device. Mounting of silicon crystals based on the principle of three-dimensional crystal assembly (3D-technology) allows solving these problems to a large extent. One of the main directions in the development of 3D integration technologies is the Through Silicon Vias (TSV) method. Such vertical system integration with the formation and subsequent metallization of vias in silicon by sputtering, chemical or galvanic deposition of metals from solutions, allows a higher packing density with a comparable wafer size, achieving greater functionality and better characteristics. This technology provides not only an increase in the degree of integration, but also reduces the complexity of the assembly, as well as improves the performance and power consumption of systems [1–3].

Aluminum is an unsuitable material for 3D technologies due to degradation processes caused by electromigration. Copper is the most promising material for interconnections due to a number of advantages over aluminum, such as lower resistance, durability to electromigration, and higher switching speeds of IC elements [4, 5]. When choosing a material and a method for its deposition, it should be keep in mind that technologically fabrication of metallization and integrated circuits mounting is a complex multistage process, including sequential deposition of various materials (metals) films onto silicon wafers, each of which performs certain functions. The requirements for such sequentially deposited layers are complex and diverse. The most important requirement is good adhesion to the polished surface of silicon wafers and to each other, small grains size, absence of pores, homogeneity, and uniform thickness.

Traditionally, under the manufacturing of three-dimensional micro- and nanostructures, metals are deposited onto a silicon substrate by chemical vapor deposition (CVD) and physical vapor deposition (PVD); however, these methods are expensive. An alternative method is an electrochemical deposition (ECD), which can be implemented as a cost-effective low-temperature process that possesses all the advantages of electrochemical processes: high speed, low cost of reagents, low energy consumption, and the possibility to process large-area substrates and complex profiles [6, 7].

Regardless of the technique to fabricate films, direct deposition of copper on silicon is unacceptable due to the diffusion and electromigration of copper atoms into silicon. In addition, direct electrochemical deposition onto a silicon substrate from traditionally used solutions is a problematic technological operation due to the poor wettability of the smooth silicon surface. Optimization of this process would make it possible to reduce the number of layers on silicon

wafers, the operations of their preparation and the required materials, that is, it would significantly simplify formation of three-dimensional Cu/Si/ SiO_2 microstructures with vias.

Usually, initially, barrier layers of silicon nitrides, silicon dioxide, titanium, titanium nitride, or nickel and its compounds with phosphorus and tungsten are formed on silicon. Some of them (nickel or its compounds) also function as an adhesive to strengthen the adhesion of metal films to an extremely smooth substrate surface [8]. Earlier, in the technology of copper metallization, it was proposed to deposit copper electrochemically on a barrier layer pre-coated with a thin seed layer formed by PVD or CVD methods [9–11]. However, as the grooves and holes sizes decrease, it becomes more difficult to deposit a continuous and defect-free seed layer. In addition, when the size is reduced to less than 100 nm, the seed layer becomes a significant part of the metallization. As a result, new strategies (variants) of direct copper deposition onto a TiN barrier layer without a seed coating (seedless copper electrochemical deposition, SECD) were proposed [12–14].

Direct electrochemical copper deposition (SECD) on the surface of a diffusion barrier layer of TiN, Ta, TaN, etc., without a copper seed coating may become the technology of the next generation of devices of ultra large-scale integration (ULSI). This option reduces the cost of manufacturing metallization and improves the quality of filling contact junctions and grooves (the ability to fill narrow channels). Depending on the chemical composition of the electrolyte, especially pH, and deposition conditions (deposition potential), copper deposits on diffusion barriers have different variants of nucleation and growth.

In addition, the presence of narrow vias in a substrate with Si/SiO_2 oxide layer leads to a change in the diffusion conditions during deposition. This is due to the inhomogeneous distribution of the current density, which is many times higher at the edges of the vias than in depth. As a result, during deposition (especially during conformal filling), narrow blind vias become overgrown with the formation of voids, which can lead to the failure of metallization systems during the IC's operation.

The aim of this study is to investigate the influence of the method of preparation (activation) of the surface of an Si/SiO_2 substrate with blind vias and the conditions of direct electrochemical deposition of copper into vias with a TiN barrier layer at the bottom of the vias on the microstructure, the nature of the interface, and the surface in the silicon–matrix system of copper columns. Such studies will simplify the technology of making vias in ICs and diversify the processes of forming various microstructures and combined nanomicrostructures based on copper columns in an Si/SiO_2 substrate.

EXPERIMENTAL

KEF-1.5 (100) monocrystalline phosphorus-doped *n*-type silicon wafers with a resistivity of 10.5 Ohm cm were used as the initial substrates. The subsequent deposition of continuous Ti and TiN layers, as well as the formation of a matrix of ordered vertical vias in silicon oxide, a barrier layer at the bottom of the vias, and a mask on the wafer surface (TiN), were carried out at JSC INTEGRAL in an Endura 5500 PVD vacuum-type cluster setup from Applied Materials as described in the patent [15].

Rapid heat treatment (RHT) to form titanium silicide at the Si/Ti interface was performed on the Heatpulse 8108 unit produced by AG Associates. As a result of annealing the Ti film on Si in a nitrogen atmosphere, the $Si/TiSi_2/Ti/TiN$ structure was formed. The method allows the formation of films of titanium disilicide of the C54 modification with a high level of electrical conductivity. This excludes the formation of the C49 type modification with low electrical conductivity.

This technology provides the formation of blind vias of different diameters in the SiO_2 layer (see below) in the form of truncated cones with a TiN barrier layer at the bottom [15]. TiN films have good adhesion to silicon and, in addition, are hard, chemically inert, and thermodynamically stable.

The diagram and appearance of a fragment of the original test structure (experimental sample) with a matrix of blind vias are shown in Fig. 1. One substrate contains four modules with an array of vias of different diameters: 500, 1000, 1500, and 2000 nm.

The *n*-Si/TiN contact through the $TiSi_2$ thin layer is practically ohmic, and this structure provides good electrical contact with the TiN thin layer. However, in order to avoid possible limitations in the processes of electrochemical deposition of copper into the narrow vias related to the presence of a TiN film on the bottom of the vias, and to achieve a more uniform potential distribution over the sample surface, an ohmic contact was additionally made on the back side of the silicon wafer in some samples. A copper film 0.5 μm thick was deposited by magnetron sputtering on the back side of the substrate.

Before the electrochemical deposition of copper, silicon wafers with a matrix of vias of different diameters were activated, by varying the conditions of this stage, in a buffer solution containing $HF : NH_4F : H_2O$ = 1 : 2.5 : 5 in volume ratios at room temperature. This solution is commonly used to remove natural oxide from the surface of silicon wafers. In a series of experiments, the wafers were not processed. It was assumed that such a procedure is necessary to change the surface roughness of the TiN film to obtain a more developed surface, and, in addition, it affects the properties of the surface of the walls (SiO_2) of the vias.

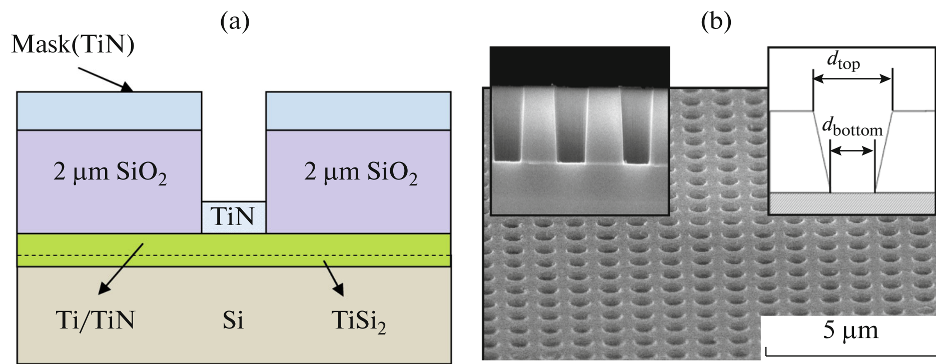

Fig. 1. Schematic representation (a), SEM photographs of the surface (b), and cross section (inset) of a fragment of the original experimental sample (module with a hole diameter of 500 nm).

It is also known that titanium oxides can form in the titanium nitride layer during RHT due to the interaction of titanium both with the oxygen in the titanium nitride in the form of a solid solution and with the oxygen entering titanium nitride from the environment. In addition, the surface of titanium nitride contains organic impurities formed in the process of obtaining a matrix of vias [16]. Therefore, such a procedure (activation) is necessary to remove oxides and organics from the surface of the barrier layer.

Further, immediately after washing in running and distilled water for 2–3 min at 22°C, the electrochemical deposition of copper was carried out directly onto the barrier layer in a sulfate electrolyte (no. 1) or in a pyrophosphate electrolyte (no. 2), the compositions of which are given in Table 1.

The standard glass two-electrode cell was used. The working electrode was an *n*-silicon substrate, which was rigidly fixed in a specially designed holder.

The metallization of the back side of the substrate and the design of the holder ensure the uniform potential distribution over the entire surface of the sample. A plate made of pure (chemically pure grade) pyrolytic graphite with the size exceeding the sample's surface area in contact with the electrolyte was used as the cathode. The use of an inert (insoluble) anode avoids changes in the concentration of nickel in the electrolyte, which makes it possible to maintain the metal's current output at the given level. The electrolyte was stirred with a magnetic stirrer.

The thickness and microstructure of the electrochemical deposit (copper) were controlled by changing the electrode potential and the time of the process. The potential was set in the linear scan mode gradually from zero to a constant value at 30 mV/s, and then maintained constant for a certain time. The current does not appear immediately but when a certain potential value is reached, which depends on the state of the sample surface (processing time and electrolyte). The measurement errors were not more than 1 mV in the potential and 30 nA in the current.

The microstructure, surface morphology, and cross section of the SiO_2/Cu (via's walls) and Si/$TiSi_2$/TiN/Cu (via's bottom) structures were studied by scanning electron microscopy (SEM) at different stages of fabrication. A Hitachi S-7800H scanning electron microscope was used at the normal orientation of the electron beam and at an angle to the surface; the magnification reached 130000× with a resolution of ~10 nm. The peculiarities of the localization of the metal phase in the SiO_2 vias and its emergence on the SiO_2 surface were studied on the sections of the samples obtained by cutting and polishing the surface with a focused ion beam using a LYRA 3 TESCAN microscope; the maximum magnification was 150000×. The chemical analysis of the elemental composition of the

Table 1. Parameters of electrolytes used for electrochemical deposition of copper

Electrolyte	Content	Concentration, g/L
No. 1	Copper sulfate ($CuSO_4 \cdot 5H_2O$)	180
	Sulfuric acid (H_2SO_4)	40
	Hydrochloric acid (HCl)	0.02
No. 2	Copper sulfate ($CuSO_4 \cdot 5H_2O$)	225
	Potassium pyrophosphate ($K_2P_2O_7$)	15

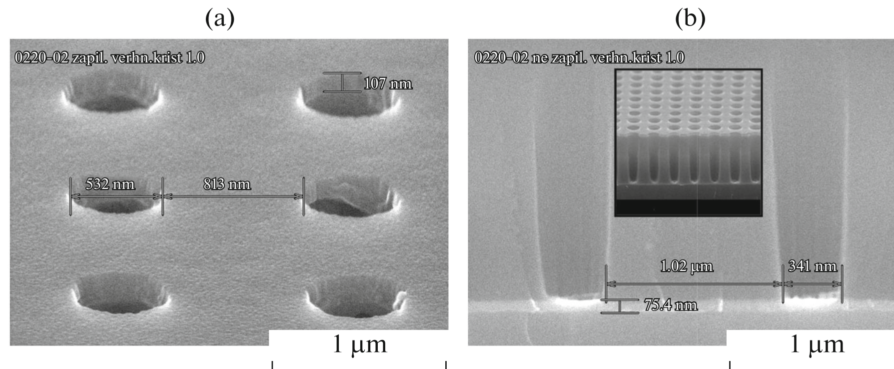

Fig. 2. SEM images of the surface (a) and chip (b) of a fragment of the initial test structure of the sample with a via diameter of 500 nm and a depth of 2.0 μm.

experimental samples was carried out on the same device with an attachment for energy dispersive X-ray spectroscopy (EDX) at an accelerating voltage of 10 kV (microanalysis system for QUANTAX 200 scanning electron microscopes, Zeiss A.G., Bruker). The depth of the analyzed layer was ~1.5 μm.

RESULTS AND DISCUSSION

Topological Features (Morphology) of the Matrix of Holes

In order to elucidate the features of the process of filling deep vias in dielectric and evaluate the obtained experimental results, we first studied the morphological features of the initial matrix (a template made of silicon oxide). Figure 2 shows SEM photographs of the surface and a cross section of the initial silicon structures.

As can be seen from the photographs, the morphology (shape) of the vias, which is determined by the pattern of the photolithographic mask, is quite regular and uniform. The vias depth is 2000 ± 50 nm and is determined by the thickness of the SiO_2 dielectric layer. The distribution of the vias diameter along the depth is trapezoidal; the walls of the vias are smooth. The thickness of the titanium nitride mask on the sample surface is 110 ± 10 nm; the thickness of the barrier layer at the bottom of the vias is ~80 ± 10 nm.

Morphology of SiO_2/Cu and Si/$TiSi_2$/TiN/Cu Structures

The state of the surface of SiO_2/Cu and Si/$TiSi_2$/TiN/Cu structures, after deposition of metal into the vias without precursive processing, was preliminarily assessed by the optical microscopy method. The express analysis showed that, as a result of the electrochemical deposition at a potential of −1.6 V for 5 min, copper is localized only in the areas of some vias. A continuous copper film is not formed on the surface. A detailed SEM analysis of the chips of the same samples showed that copper is deposited in almost all the vias, albeit, unevenly (see Fig. 3).

Some vias are filled with metal in excess (Fig. 3), while in others Cu is visually absent (Fig. 3a). To establish the presence or absence of deposit in such vias, X-ray spectral analysis was carried out along the line passing over the visually unfilled areas (Fig. 4).

Copper reflections are not recorded in all vias but only in those that appear filled or half-filled on the SEM image of the chip (Fig. 3b). This is partly due to the fact that the depth of the analyzed layer is less than 1.5 μm; however, there are also empty vias. On SEM photographs of the surface, Fig. 3a, the caps are clearly visible only above the completely filled vias.

Analysis of the SEM photographs of chips in several areas 80 μm long shows that at the initial stage most of the vias are filled. It is possible that some of them are blocked by hydrogen bubbles during the deposition process. Another reason for the uneven deposition of copper into the vias is most likely due to the peculiarities of the electrochemical deposition of copper on the smooth surface of the poorly wetted TiN barrier layer.

The results of the SEM study of chips of the treated samples of SiO_2/Cu and Si/$TiSi_2$/TiN/Cu are shown in Fig. 5. It can be seen from the photographs that under identical deposition conditions (electrolyte no. 2, potential −1.6 V, deposition time 5 min), the metal is deposited into all the vias and emerges on the surface. A more intense lateral growth of copper agglomerates occurs above the mask surface.

The resulting copper columns have axial symmetry, repeating the shape of the vias. It can be seen from the photographs that during the chemical treatment of the samples, the walls of the silicon oxide vias are etched unevenly. The bottom area of the vias is slightly wider. This is due to the fact that silicon oxide consists of two layers: the bottom layer is an oxide obtained by CVD, with a thickness of 0.6 ± 0.05 μm. The upper layer is an oxide obtained by plasma enhanced chemical vapor deposition

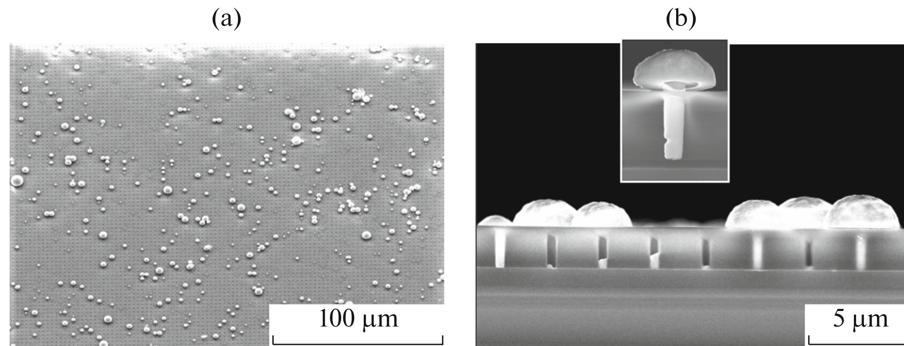

Fig. 3. SEM images of the surface (a) and chip (b) of the structures of SiO_2/Cu (via's walls) and Si/$TiSi_2$/TiN/Cu (via's bottom).

(PECVD), with a thickness of 1.4 ± 0.07 μm. The thermodynamic nonequilibrium of the decomposition processes in a gas discharge during PECVD allows the deposition of SiO_2 and other dielectrics at lower temperatures than in similar CVD processes with thermal decomposition of the reaction gas [17]. As a result, the PECVD oxide exhibits a higher chemical resistance in the buffer solution, which is designed to treat the bottom of the vias, and the CVD oxide is etched (dissolved).

Thus, the morphology of copper columns in vias is determined to a greater extent by the process of matrix fabrication (including the activation stage) than by the process of electrochemical deposition. In this embodiment, with the activation of the surface of the barrier layer, copper is deposited in all the vias evenly and up to the surface.

It is important to note that the titanium nitride is not etched in the buffer solution used. It is generally difficult to etch it chemically and it is usually removed (or thinned out) by ion etching. It is clearly seen in the insets in Figs. 5c and 5d, that the titanium nitride (TiN) layer remains at the bottom of the vias, and a thin layer of titanium disilicide ($TiSi_2$) is also visible on the continuous TiN layer. The formation of a wetting Cu layer is also not excluded, since the thickness of the interlayer at the bottom of the vias is somewhat greater than the thickness of the initial TiN layer.

When the wafers are chemically treated, the surface of the mask also changes; it becomes rougher. As a result, a more intense lateral growth of copper agglomerates occurs above the mask surface than in the first case.

To study the conditions for the nucleation of copper on the surface of the barrier layer, microstructures were fabricated with partial filling of the vias with metal at a potential of –1.6 V, albeit, for a shorter time (2 min). Figure 6 shows the SEM images of the copper crystallites at the initial stage of deposition.

At a higher magnification, it can be seen that the surface of the copper particles is not smooth, since they consist of separate clusters adjacent to each other. Crystals of various shapes, 100–200 nm in size (Figs. 6a, 6b), at high magnification represent chains of crystallites ~30–50 nm in size (Fig. 6d).

It is well known that only in exceptional cases a crystal is formed in a geometrically regular shape as a regular polyhedron or polyhedron. This occurs when the external conditions favor the full development of the crystal (in all directions). The photographs illustrate the tendency of copper to form deposits in the form of irregular polyhedrons of various shapes in vias

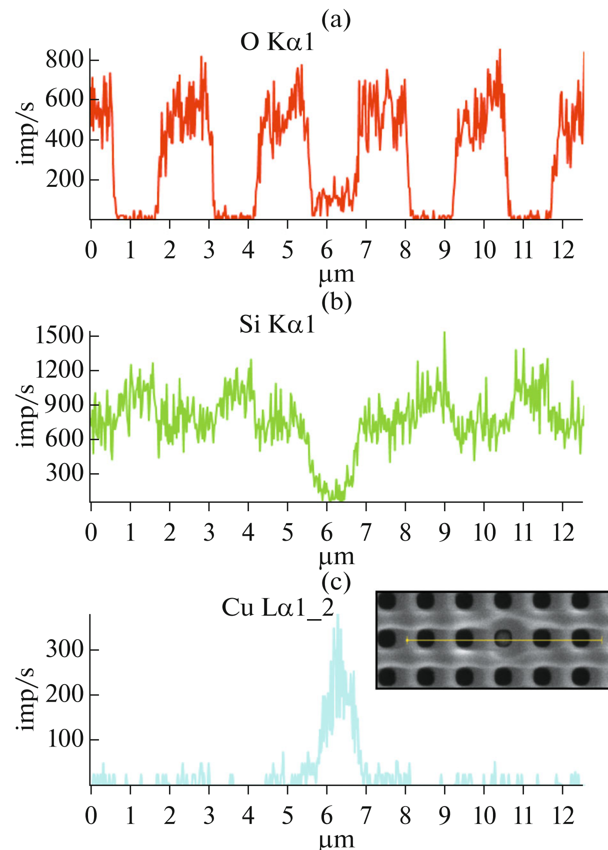

Fig. 4. Results of X-ray spectral analysis of the SiO_2/Cu and Si/$TiSi_2$/TiN/Cu structures along the indicated line.

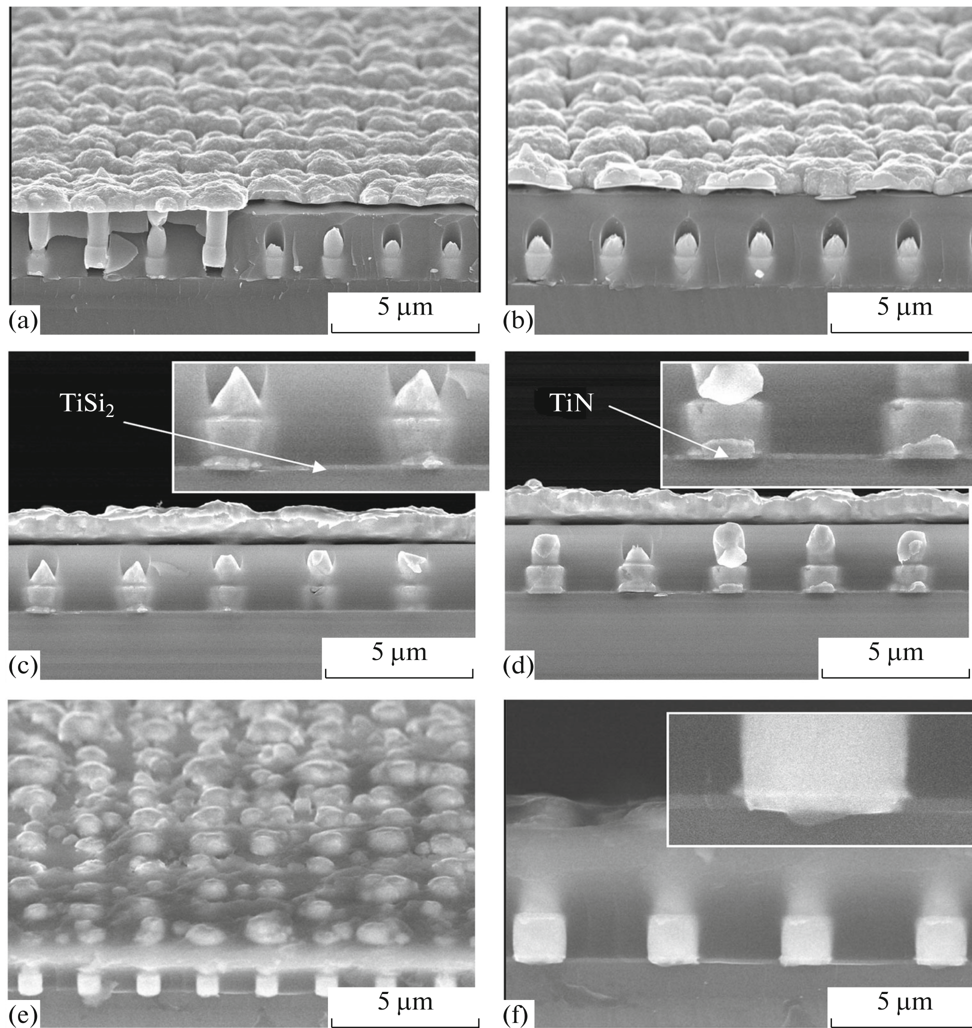

Fig. 5. SEM images of chips of SiO_2/Cu and Si/$TiSi_2$/TiN/Cu structures for three identical (0.5 × 2.0 μm) samples for (a, b) processing time 20 s, (c, d) processing time 30 s, and (e, f) processing time 25 s.

with a diameter of 2.0 and 1.5 μm. Under conditions of limited space (especially in vias with a diameter of 1.0 and 0.5 μm), crystals of irregular shape are formed, the crystallites of which have a branched shape with empty spaces, resembling a tree (dendrites); Figs. 6c and 6d [18]. A comparison of the photographs in Figs. 6b and 6c suggests that the smaller the vias diameter the higher the probability of dendrite formation. Further, the treated vias are completely and uniformly filled by copper with practically the same lateral dimensions. The filling rate depends on the type of electrolyte, processing time, and via' diameter.

Thus, it was found that the activated TiN layer, which does not contain oxides after treatment, is suitable for the seedless deposition of Cu into vias with a diameter of 500 to 2000 nm. The deposition on the TiN surface with a reduced content of oxides (and organic impurities) leads to the formation of a wetting Cu layer (Fig. 5d), to a faster coalescence of the nuclei, and an improvement in the adhesion between Cu and TiN.

Peculiarities of the Process of Electrochemical Deposition of Copper into Vias with a Barrier Layer at the Bottom

Depending on the composition of the electrolyte and the modes of copper deposition into vias with high aspect ratio, two types of filling can be observed: conformal and bottom-up. Conformal and superconformal filling (along the walls of the vias) is achieved by special additives that inhibit deposition on the ridges and accelerate the growth of copper in the grooves. In this case, cavities can form in the interlevel vias with high aspect ratio (a.r.) greater than 5, which increase the resistance of the conductors and, at high current densities, can lead to the failure of metallization systems during the operation of the circuits. Another option for filling without voids is bottom-up filling.

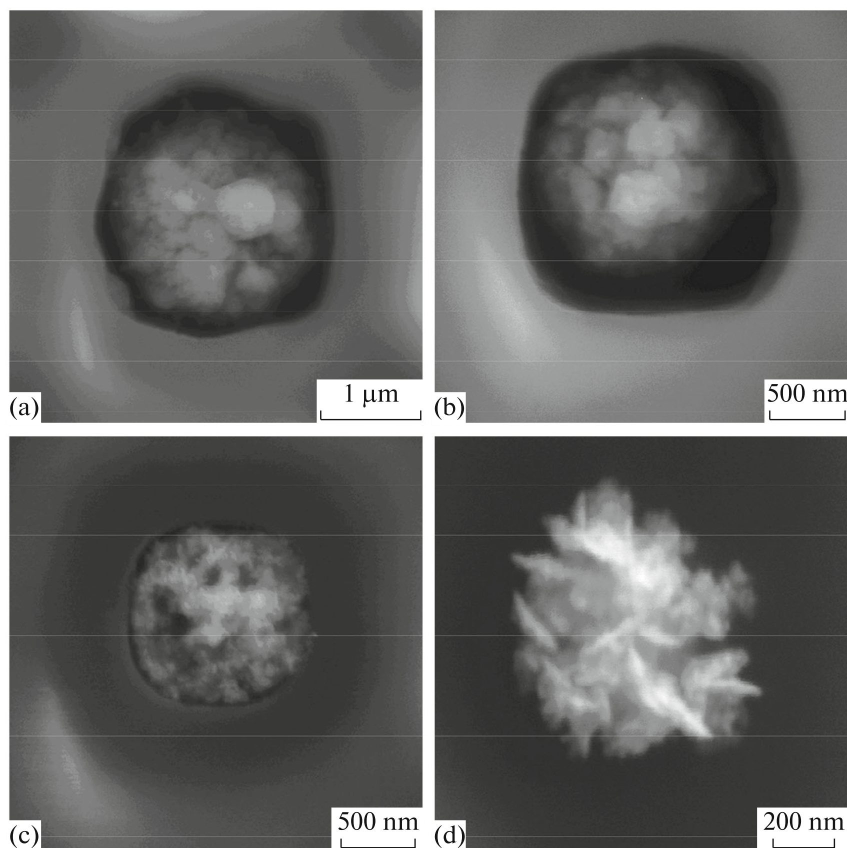

Fig. 6. SEM images of the structure of the metal deposit after 2 min electrochemical deposition of copper in electrolyte no. 2 into vias of different diameters: (a) 2.0 μm, (b) 1.5 μm, (c) 1.0 μm, and (d) 0.5 μm.

In our case (a.r. less than or equal to 4), the use of complex electrolytes is economically and technologically inexpedient. We used the second option and the two most well-known electrolytes in copper electroplating.

Since cathodic deposition can only take place on a conductive surface, when current is passed, the electrolyte's molecules are initially evenly distributed only at the bottom of the pretreated via. In the process of growth from bottom to top in a limited space, the electrode surface area inside the window does not change, and the diffusion of copper ions is accelerated (simplified). This leads to an increase in the deposition rate at the center of the window. The accelerated growth of the film in the center of the window leads to the formation of a protrusion, first above the metal column and then above the via (Fig. 3). The same protrusions are formed during superconformal filling [19].

The presence of a protrusion on the electrode surface inevitably leads to an inhomogeneous distribution of the electric field strength. In the vicinity of the protrusions with a small radius, the field strength increases. Since the ions are delivered jointly by electromigration and diffusion, a relief develops (rapid spreading of copper over the sample surface).

This effect can be minimized by adding a background electrolyte containing highly mobile cations [20]. Sulfuric acid (H_2SO_4) is most often used as the background electrolyte in copper deposition. The mobility of H^+ ions significantly exceeds the mobility of Cu^{2+} ions. Therefore, the former make the main contribution to the drift current, while the latter move to the electrode mainly through diffusion.

In addition to the background additives, copper's deposition electrolytes contain components that affect the character of the deposition reaction due to adsorption on the cathode. For example, buffer additives that ensure a constant pH value contain Cl^- ions, which activate the formation of planes oriented in the [100] direction. This leads to the formation of the characteristic relief of the coating, which consists of cubic crystallites or dendrites. Both of these additives are present in electrolyte no. 1.

The electrochemical deposition of thin copper films on a flat substrate surface is carried out, as a rule, at a constant potential close to the equilibrium potential of the deposition of the given metal in the given electrolyte, which is close to zero for copper. During electrochemical deposition into a porous matrix (through long narrow channels), the supply of a fresh

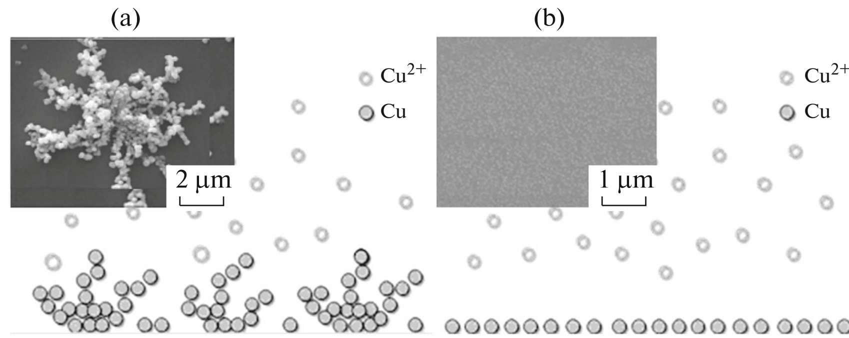

Fig. 7. Schematic representation (model) of the formation of copper deposits depending on the deposition potential [21]: (a) at a potential of –0.5 V vs. Ag|AgCl, and (b) at a potential of –0.25 V vs. Ag|AgCl.

electrolyte (electrolyte circulation) to the barrier layer is hampered, and, in addition, the pores may be clogged with bubbles of the evolved hydrogen at high potentials (more than equilibrium).

The influence of various intermediate layers on the potential for electrochemical copper deposition has been discussed in a number of works. In [21], a possible mechanism of the growth of copper films on the surface of a glass substrate coated with ITO (indium tin oxide) at various deposition potentials was investigated. The results of this study showed that at more negative deposition potentials in a three-electrode cell, tree-like particles are formed, rather than a continuous film, Fig. 7.

The optimal conditions for the deposition of copper films on a flat surface of the TiN layer were described in [22]. The aim of the experiment was to obtain copper nuclei with a high density, uniform size, and hemispherical shape. A good result was obtained at deposition potentials in the range from –0.5 to –1.0 V relative to the Ag/AgCl reference electrode (in a three-electrode cell). The traditionally used potentials close to zero (for copper) led to the formation of needle-like crystals of inhomogeneous size (–0.15 V) or nodular spheroidal particles (–0.25 V). In both cases, the concentration of nuclei is much lower than at a potential of –1.0 V. Similar studies on the direct deposition of copper in vias with a barrier layer were not found in an open print.

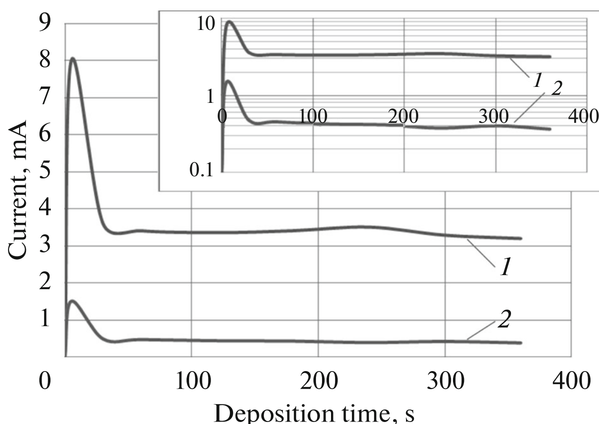

Fig. 8. Dependence of the electrochemical deposition current on the deposition time and type of electrolyte: (*1*) electrolyte no. 1 and (*2*) electrolyte no. 2.

Guided by the experience of applied galvanics and the analysis of the published data [23–25], we used two well-known (typical) electrolytes: sulfate (no. 1) and pyrophosphate (no. 2). Chlorine ions (0.02 g/L HCl) were introduced into the sulfate electrolyte. The deposition process was carried out in an easy-to-use two-electrode cell at the same constant potential in both electrolytes. The deposition mode (deposition potential) was determined experimentally for these conditions (two-electrode cell) and the type of samples—not a flat surface, as in planar deposition, but a matrix with blind, sufficiently deep (2000 nm), and narrow (500 nm in diameter) vias, at the bottom of which a barrier layer exists.

Taking into account the known results [21, 22, 26, 27] and our own experience of working with a two-electrode cell, deposition was carried out at a constant potential close to –1.6 V (1.6 ± 0.25 V).

Figure 8 shows the dependences of the current (current density)[1] on deposition time and type of electrolyte after preliminary treatment of the samples for 20 s. Figure 9 shows the dependences of the current on deposition time in electrolyte no. 2 at a potential of –1.6 V before (*4*) and after (*1*, *2*, and *3*) sample treatment at different deposition times.

An analysis of these dependences shows that the deposition rate, which is proportional to the current density, depends on the type of electrolyte to a greater extent than on the sample surface treatment time. Moreover, in the first electrolyte, it is much higher than in electrolyte no. 2.

A sharp change in the current when the metal columns emerge is not recorded. One substrate contains four modules with a matrix of holes of different diameters. Vias with a diameter greater than 500 nm were

[1] The visible surface area of all samples is the same.

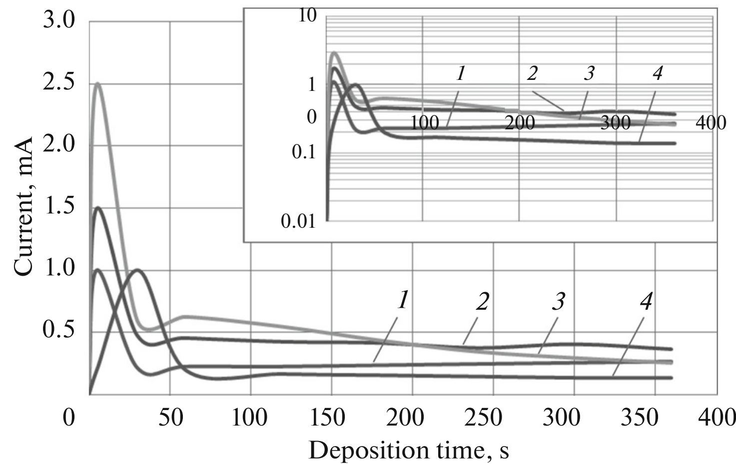

Fig. 9. Dependence of the electrochemical deposition current on the deposition time and on the processing time: (*1*) 10 s, (*2*) 20 s, (*3*) 30 s, and (*4*) without treatment.

filled slower and gradually, which made it difficult to control the process by the current. The larger the via's diameter the slower it was filled; thus, the current barely changed since all vias of different diameters were gradually filled.

This is in good agreement with the assumed bottom-up column growth model discussed earlier (see above). The increase in the deposition rate when approaching the surface leads to a rapid spreading of copper over the entire surface of the sample. This is an undesirable effect[2] that cannot be controlled by timely switching off the cell (stopping the deposition process). Therefore, the deposition rate, which is higher in the first electrolyte, does not play a decisive role in this process. The main requirement is a controlled uniform deposition into all vias without voids; it is performed at a lower filling rate, i.e., in electrolyte no. 2. Thus, the results obtained show that, firstly, 15–20 s of treatment in the solution used is sufficient, and, secondly, electrochemical deposition is best carried out in pyrophosphate electrolyte no. 2.

CONCLUSIONS

The morphological features of $Si/SiO_2/TiN/Cu$ and $Si/TiSi_2/TiN/Cu$ nanostructures fabricated by the local electrochemical deposition of copper in conventional industrially used copper plating electrolytes were investigated.

It was found that under certain conditions of activation of silicon wafers by treatment in the used buffer solution, uniform (without voids) copper columns with good adhesion to the barrier layer are formed.

The mode of direct electrochemical deposition of copper on the surface of the barrier layer into the vias of the silicon wafers was selected, which makes it possible to carry out the 100% (in all vias) deposition of metal without internal voids. At the same electrochemical deposition potential (–1.6 V) in electrolyte no. 2, an almost uniform metal deposition occurs, which makes it possible to control the degree of filling by changing the deposition time.

Structures with vias partially or completely filled (with caps over the SiO_2 surface) were created. The morphological studies of structures with partially or completely filled vias showed that copper clusters consist of tree-like crystallites ~30–50 nm in size.

The fabricated experimental silicon crystals with the blind vias of an ordered shape and insulation on the surface of these vias meet the requirements for structures used to implement three-dimensional metal interconnections of ICs based on them [28]. In addition, arrays of ordered microvias in silicon can be used in electronics to manufacture capacitors of increased capacity [29] and photonic crystals [30], and also as microchannel plates for electron multipliers [31].

[2] Copper is usually removed from the surface by polishing the sample, which is an additional operation.

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