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CODEC FOR TWO-DIMENSIONAL HAMMING CODE ON FPGA

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Annotation. This work demonstrates a high-performance FPGA implementation using VHDL. The implementation includes multiple error detection and correction algorithms of Hamming product code variants, and includes selectable features such as hybrid automatic repeat request and parallel coding.

Keywords. FPGA, error correcting code, hamming code, product code.

In digital communication systems, errors can occur during data transmission due to noise, interference, or other factors. Error correcting codes are used to detect and correct these errors, ensuring the accuracy and reliability of digital communication. One popular error correcting code is the Hamming code, developed by Richard Hamming in the 1950s.

Hamming code works by adding extra parity bits to the original data bits. This creates a unique pattern of 1s and 0s that can detect and correct errors that may occur during transmission. The parity bits are added in a way that creates a unique pattern for each possible combination of single-bit errors that might occur during transmission. When the receiver receives the code, it checks the parity bits and compares them to the expected pattern. If there is an error, it can use the unique pattern to determine which bit has been flipped and correct the error.

The 2D Hamming code, also known as the Hamming product code, is an extension of the original Hamming code that is used for error detection and correction in two-dimensional arrays of data. This code adds extra parity bits to each row and column of a two-dimensional array, allowing it to detect and correct errors that may occur in both the horizontal and vertical directions. The 2D Hamming code is particularly useful in applications that require reliable transmission of data in two-dimensional formats, such as image or video data.

In this work, we implemented the Hamming product code on a Field Programmable Gate Array (FPGA). Our implementation is in a modular design, the overview of the whole system is shown as Figure 1. below.

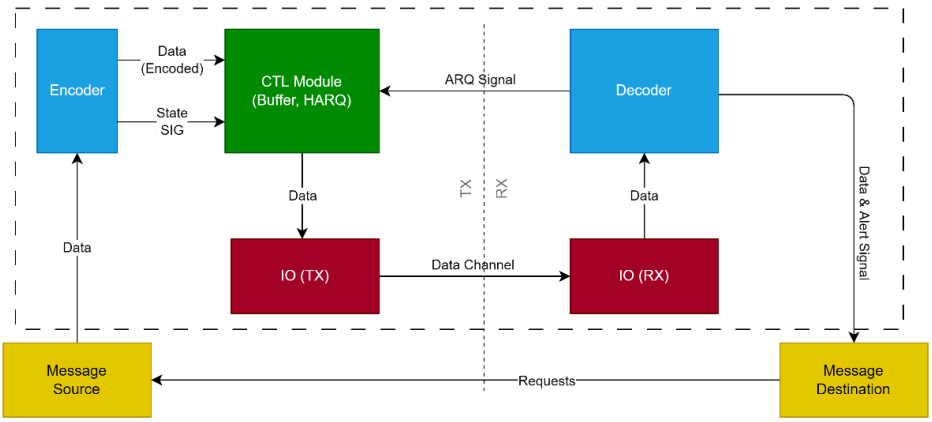

Figure 1 - System modules and structure block diagram

The decoder module plays an adapter of different algorithm, for now, the implementation come with 3 different algorithms: BaoV3, SHPC, EHPC. The different decoder algorithm has different extra feature support shown in Table 1 below.

Table 1 - Algorithm unit performance and capability

Algorithm	Codeword	Error Correcting	HARQ
BaoV3	8 Bit	4 Bit	Support
SHPC	8 Bit	4 Bit	Optional
EHPC	7 Bit	3 Bit	Optional
Encoder	8 Bit	4 Bit	-
Encoder	7 Bit	3 Bit	-

The design of this system supports installation multiple parallel workers to accelerate the decoding process. Table 2 below shows the unit resource usage and a typical performance at Fmax, which is an estimated value from four types of FPGA typical working conditions: combination of 0℃ and 85℃ at 1100mV. The average speed is calculated from the total clock cycles and the typical Fmax.

Table 2 - Algorithm unit resource usage

Algorithm	Logic utilization (in ALMs)	Total registers	Fmax	Avg. Speed
BaoV3	278	120	95 MHz	13 MB/s
SHPC	882	224	45 MHz	6.1 MB/s
EHPC	753	215	60 MHz	8.1 MB/s
ENCODE	70	141	300 MHz	40 MB/s
ENCODE	68	135	350 MHz	47 MB/s

Reference:

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