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Chapter 1. Assembly and Mounting of Electronic Devices: Advancements in Technology and Equipment

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Abstract—This chapter explores the evolving trends in contemporary electronic module designs and assembly technologies. The enhancement of computer technology and digital communication tools, coupled with the escalation in the operational speed of the elemental base, hinges directly on the reduction of signal transmission length between logical elements, i.e., the constructive delay of the transmitted signal. Interconnection technology, crucial for bridging the microcosm of semiconductor chips with the external world of electronic devices, emerges as pivotal for producing viable products. We provide a comprehensive classification and discussion of assembly connection designs, employing methods involving direct material contact under the influence of pressure, heat, and physical impact in various combinations. Intermediate materials such as solder, microwires, and conductive adhesives are utilized in these processes. Special emphasis is placed on surface mounting of electronic components, COB assembly technology, Flip Chip, BGA, and the assembly of multichip electronic modules.

Keywords: designs, technology, assembly, mounting, electronic modules

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1. TRENDS IN THE DEVELOPMENT OF ELECTRONIC MODULES

Assembly and mounting operations remain the most labor-intensive aspects of electronic device manufacturing, constituting up to 50–70% of the total labor input in production. The miniaturization of components and the development of functionally complex microelectronic devices, particularly very large-scale integrated circuits and microprocessors, have posed specific challenges in the field of microassembly of electronic devices. A yearly average increase of 75% in the density of active elements on a chip necessitates a 40% annual rise in the number of leads on packages [1]. This drives a continually growing demand for novel encapsulation methods, fostering high-density interconnections on printed circuit boards. Achieving high functional complexity and integration levels is unattainable without significant enhancements to the contact connection system. The development of microprocessors with signal operating frequencies up to 5 GHz escalates the lead count to 1000 [2].

The adoption of multichip modules (MCMs), i.e., thin-film multilayered hybrid structures fabricated on ceramic, silicon, or metal substrates, to which chiplets are attached by welding or soldering, has increased the density of mounting connections to 200 per square centimeter [3]. Conventional assembly processes fail to deliver the currently required high productivity and high yield percentage of fully assembled products with dense mounting. Statistical data reveals that 50–80% of all failures in electronic systems occur due to connection defects, and the cost of detecting and rectifying a failure at the block assembly stage is 100 times cheaper than during equipment testing [4].

According to the International Technology Roadmap for Semiconductors (ITRS), the industry is transitioning to 450-mm wafers, introducing silicon-on-insulator (SOI) structures, increasing metalization layers to 14, shifting to low-temperature assembly processes (below 200°C) using through-silicon vias, increasing the number of package pins to 5000 and more with a pitch of matrix pins down to 0.2 mm, and transitioning to frequencies in the range of 10–100 GHz [5].

Several components stand out within the structure of electronic systems, including the packages, electronic modules assembled using various elements such as transistors, integrated circuits, resistors, capacitors, as well as switching devices, information display means, and others. The market demands more functionalities in smaller, faster, and more cost-effective devices, which are assembled within the packages of integrated circuit types such as CSP, BGA, PLCC, SOIC, and SOP, among others. In modern electron-

ics, intensive efforts are being made towards further miniaturization and integration of produced items, particularly in the high-frequency and microwave sectors, associated with the rapid development of telecommunication technologies, aerospace engineering, and instrumentation [6].

The main trends in the development of electronic modules include

– Increase in operating frequencies and enhancement of digital information processing speed in electronic systems;

– Growth in the number of inputs/outputs and the increase in component density on the board;

– Micro-miniaturization of electronic components, transitioning from 2D to 3D module structures;

– Rise in power consumption and challenges associated with heat dissipation in electronic modules;

– Ensuring electromagnetic compatibility of electronic modules.

At a certain stage, the increase in component density within the volume of electronic devices adhered to Moore's Law (1965), which stated that the number of transistors in integrated circuit (IC) memory doubles every 18 months. In 1975, Prof. Moore reformulated his law, noting that the scaling time (i.e., the transition to the next technological generation) had increased to 2 years. He identified factors determining the scaling process:

– Increase in chip area;

– Higher density of component placement and decrease in their sizes;

– Advancement in device and circuit intelligence;

– Enhanced production efficiency, achieved through increasing the diameter of processed wafers to 300 mm or more.

The enhancement of computer technology and digital communication tools, alongside the increase in the operational speed of the elemental base, is directly contingent upon the decrease in the length of signal transmission between logical elements, commonly known as the constructive delay of the transmitted signal. When comparing the switching time of logical elements, which does not exceed a few nanoseconds in modern large-scale integrated circuits, with the signal propagation time in printed conductors (6–7 ns/m), it becomes evident that the primary component of time delay in electronic products is attributable to interconnect delays,

$$\tau = \sqrt{LC} = \tau_0\sqrt{\varepsilon\mu}, \tag{1}$$

where L is the length of the connection; C is parasitic capacitance; ε is the dielectric constant of the material; μ is magnetic permeability; τ_0 is delay per unit length.

The increase in operational speed must be accompanied by the maximum possible shortening of these delays, achieved through increasing the integration level of logical elements, denser placement of microchips on boards, and shortening connection lengths. Consequently, interconnection technology emerges as a critical technology that bridges the microcosm of semiconductor chips with the external world of electronic devices.

The increase in integration level leads to a rise in the number of input (output) pins of microchips, n, following Rent's rule [3],

$$n = kN^p, \tag{2}$$

where k is the average pin-to-gate ratio; N is the number of logical elements; p is the Rent index depending on the structure of logical circuits.

In integrated circuits, for example, k = 3–4 for a two-input integrated circuit, $p < 0.5$ for microprocessor logic, and p = 0.5–0.75 for high-performance processor logic. The number of connections, N_c, is determined by the total leads across all M microchips connected to the traces of the printed circuit board,

$$N_c = k_b Mn, \tag{3}$$

where k_b is the branching coefficient of connections, depending on the number of loads m in the interelement connection circuits: $k_b = m/(m + 1)$, so $0.5 < k_b < 1.0$.

The ratios of the board area S_n to the total number of circuits N_{circ}, the product of the number of inputs/outputs of components N_{in}, and the coefficient of surface utilization of the board K_u represent, respectively, the densities of conductors and assembly,

$$\Pi_{cond} = \frac{N_{circ}}{S_n}, \tag{4}$$

$$\Pi_a = \frac{\sum N_{in}K_u}{S_n}. \tag{5}$$

K_u can be calculated as

$$K_u = \frac{\sum S_{ce}}{S_n}, \tag{6}$$

where S_{ce} is the area of mounting holes for output components and pads for surface-mounted components.

To estimate the density of mounting connections, the following equation is used [2]:

$$\Pi_c = 2.25pN_{in}, \tag{7}$$

where p is the pitch between the housings of electronic components.

Conductor density increases with the decrease in printed circuit board area and the increase in the number of interconnection circuits. To enhance assembly density, it is necessary not only to increase the density

of conductor tracing but also, more effectively, to augment the number of interlayer connections.

Technological changes in the field of printed circuit board assembly are associated with new designs of integrated circuits. Transition to surface mount technology results in that PLCC and TO packages, which constitute approximately 90% of all devices, are being replaced by PDSO and SOT23 packages. PLCC packages are replaced by PDSO when there is a large number of pins and by PQFP when there are fewer pins. The primary reasons for such replacements are the challenges in controlling soldered connections of *j*-pins located beneath the packages and the larger surface area of the printed circuit board occupied by PLCC packages.

Ceramic and plastic QFP packages are widely used for arrays of logic elements and microprocessors. The ongoing trend of hardware miniaturization leads to further cutting in package sizes, making them increasingly smaller and thinner. Ultrathin packages such as PTSOP or PTQFP with standard pin counts become a viable alternative to most high-density chip mounting methods like TAB, COB, or Flip Chip. The main challenge hindering the widespread adoption of SMD packages with pitches less than 0.3 mm is the miniature size of the pins and the need to ensure their high coplanarity. Deviation from the normal position of even one pin results in equipment failure.

One of the promising directions in chip mounting is a chip scale packaging (CSP) technology, where internal connections are made as tape-automated bonding (TAB). By using a foil film as the chip carrier and achieving pin pitches as low as 0.3 mm, results similar to those of copper frame technology can be attained. In terms of board footprint, TCP packages are comparable in size to COB and Flip Chip.

In comparison to through-hole mounting, surface mount technology generates higher thermomechanical stress in components during soldering. Reflow soldering of large-sized plastic packages may result in the “popcorn effect” due to moisture evaporation, leading to the formation of cracks in both the package and the chip.

BGA packages offer significant advantages. Products with BGA can be assembled on existing SMD assembly lines, with the distance between the pins posing no serious issues. Unlike UltraFine Pitch, solder joints in BGA are sufficiently spaced, typically at distances of 1.27 or 1.52 mm. BGA packages have smaller contact pad sizes compared to QFP and occupy 50% less board area compared to them. Unlike TAB, BGA pins are fully inspectable before assembly and do not require special equipment. BGAs are used for mounting chips with large pin counts, i.e., 86, 119, 169, 225, and 357. BGA packages can be designed with shorter interconnections, resulting in lower pin inductance, higher mechanical resonance frequency, and better power dissipation compared to QFP under similar conditions.

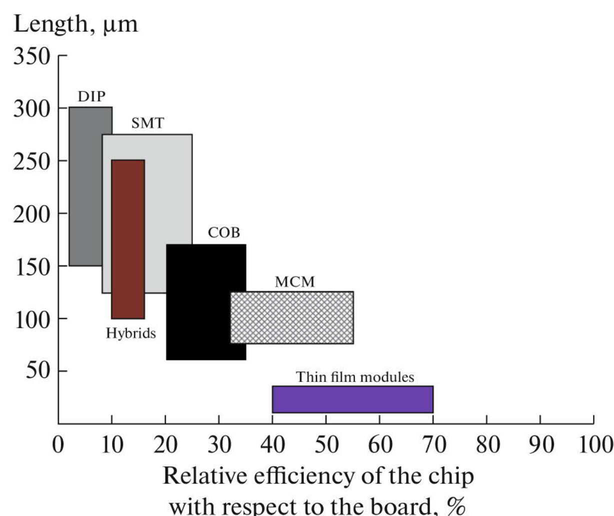

Fig. 1. Efficiency of electronic module assembly technologies.

The efficiency of electronic module layout, depending on the elemental base and assembly technology, is illustrated in Fig. 1 [7], while the evolution of IC packages and assembly technologies is shown in Fig. 2.

The common trends defining the processes of electronic module assembly in the coming years are [2]

• Transition towards more miniature, ultrafast electronic modules with increasing functionality and a short product lifecycle, making full optimization of component spectrum and printed circuit board practically impossible within the given timeframe;

• Increased integration level of components (number of input/output channels) and higher operating frequencies;

• Augmentation of the number of package pins and decrease in the minimum pitch of pins (down to 0.15 mm);

• Integration of multiple devices into a single chip or package;

• Transition of assembly and manufacturing processes from developer firms to specialized companies;

• Improvement in utilization rates and increased efficiency of assembly systems, as well as qualitative and quantitative assembly indicators, through modern software;

• Cut in the specific component assembly costs;

• Development of alternative concepts and assembly equipment to gain competitive advantages;

• Identification of rapidly developing production areas in the electronics industry: personal computers and peripheral devices (printers, modems, and network adapters); communication devices (mobile phones and smartphones, electronic modules for