ACS APPLIED ELECTRONIC MATERIALS

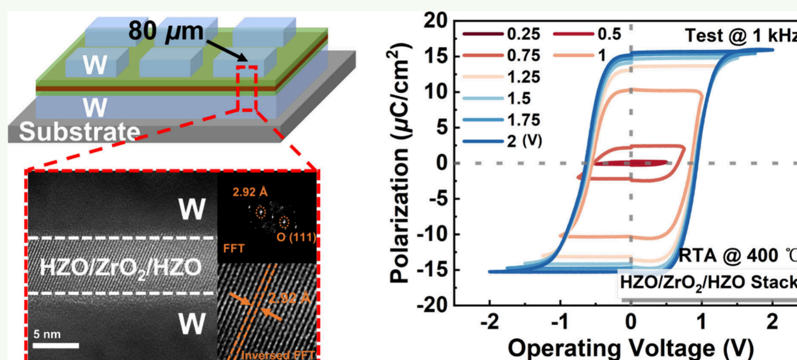
pubs.acs.org/acsaelm Article

Enhanced Ferroelectricity and Reliability in Sub-6 nm Ferroelectric $Hf_{0.5}Zr_{0.5}O_2/ZrO_2/Hf_{0.5}Zr_{0.5}O_2$ Stack Film Compatible with BEOL Process

Yinchi Liu, Jining Yang, Hao Zhang, Dmitriy Anatolyevich Golosov, Chenjie Gu, Xiaohan Wu, Hongliang Lu, Lin Chen, Shijin Ding, and Wenjun Liu*

Cite This: ACS Appl. Electron. Mater. 2024, 6, 8507–8512 Read Online

ACCESS | Metrics & More | Article Recommendations



ABSTRACT: In this work, the back-end of line (BEOL) compatible sub-6 nm $Hf_{0.5}Zr_{0.5}O_2/ZrO_2/Hf_{0.5}Zr_{0.5}O_2$ (HZO/ZrO_2/HZO) stack and the corresponding capacitors were fabricated. The capacitor with the sub-6 nm HZO/ZrO_2/HZO stack annealed at 400 °C shows a superior remanent polarization ($2P_r$) of 26.3 $\mu C/cm^2$ under only ±1.25 V sweeping, while the conventional HZO film presents nonferroelectricity. The enhanced ferroelectricity stems from the increased ferroelectric phase proportion with ZrO_2 insertion. Moreover, the capacitor with a HZO/ZrO_2/HZO stack also achieved an excellent endurance with a $2P_r$ of 27.1 $\mu C/cm^2$ after 10^{11} cycles without breakdown and only ~12% $2P_r$ degradation at 85 °C. The robust reliability is ascribed to the suppressed generation of defects and domain pinning under the low operating voltage. The sub-6 nm HZO/ZrO_2/HZO stack presents great potential for BEOL compatible nonvolatile memories in advanced process nodes.

KEYWORDS: *back-end of line, ferroelectric stack, ferroelectricity, endurance, low-voltage operation*

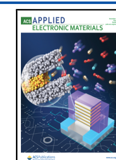
Downloaded via FUDAN UNIV on December 3, 2024 at 02:05:34 (UTC).
See https://pubs.acs.org/sharingguidelines for options on how to legitimately share published articles.

1. INTRODUCTION

As a promising candidate for high-density emerging nonvolatile memories, Zr-doped HfO_2-based ($Hf_{0.5}Zr_{0.5}O_2$, HZO) ferroelectric (FE) materials have attracted the most attention due to their back-end of line (BEOL) process compatibility as well as sub-10 nm scalability.[1−3] Extensive research has been proposed for the application of emerging memories, including ferroelectric field-effect transistors (FeFETs), ferroelectric random-access memories (FeRAM), and ferroelectric tunnel junctions (FTJs). Yet a higher operating voltage (>1.8 V) accompanied by poor endurance in the FE-HZO-based device still restrict its wide adoption.[4,5] Recently, reducing the thickness of FE-HZO films has been considered one of the most feasible and straightforward approaches to lower operating voltage and thereby high reliability in FE devices.[6] However, with the thickness scaling, the significantly increased thermal budget and persistent polarization (P_r) deterioration limit the BEOL integration. This is due to the challenge of achieving ideal ferroelectric phase crystallization quality in ultrathin HZO films during low-temperature annealing at or below 400 °C. So far, several efforts have been made to optimize the HZO crystallization by the electrode engineering[7] and interfacial layer.[8] Nevertheless, there are some trade-offs within the ferroelectricity, thermal budget, and endurance.

In addition, constructing a fine stack would also be beneficial to the crystallization of HZO thin films. Our previous work has demonstrated that an improved ferroelectric phase proportion and enhanced $2P_r$ under a low operating electric field of 2 MV/

Received: October 1, 2024
Revised: October 26, 2024
Accepted: October 31, 2024
Published: November 14, 2024



ACS Publications © 2024 American Chemical Society

cm in 10 nm FE-HZO capacitors can be obtained under 400 °C by inserting a ZrO_2 middle layer.[9] Thus, introducing the ZrO_2 middle layer into thinner FE films could be a more promising approach to improve crystallization quality, thereby realizing high performance in the BEOL process. Nonetheless, the strategy in the thickness scaling of FE-HZO films down to ~5 nm has not been proposed up to now.

In this study, the sub-6 nm HZO/ZrO_2/HZO stack and corresponding capacitors compatible with BEOL were fabricated. The device exhibits a competitive $2P_r$ of 26.3 μC/cm^2 under 1.25 V. Furthermore, excellent endurance properties and fatigue inhibition are achieved, with a stable $2P_r$ of 27.1 μC/cm^2 after 10^{11} cycles without breakdown under 1.75 V and only ~12% $2P_r$ degradation after 10^{11} cycles at 85 °C.

2. EXPERIMENTAL DETAILS

The schematic structure of an FE capacitor with conventional HZO and an HZO/ZrO_2/HZO stack are shown in Figure 1a,b, respectively.

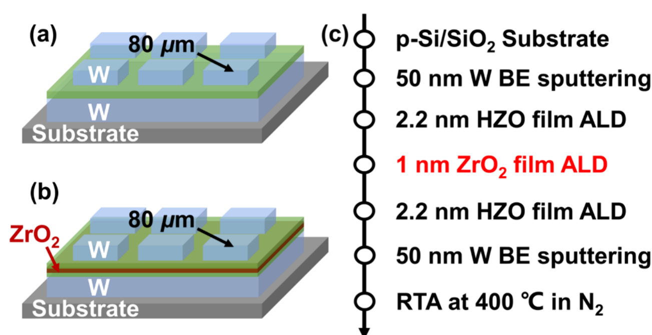


Figure 1. Schematic structure of an FE capacitor with (a) conventional HZO and (b) an HZO/ZrO_2/HZO stack. (c) Process flows of an FE capacitor with an HZO/ZrO_2/HZO stack.

The fabrication process flows of an FE capacitor with an HZO/ZrO_2/HZO stack are illustrated in Figure 1c. First, 50 nm of tungsten (W) is deposited onto the p-Si/SiO_2 (90 nm) substrate as the bottom electrode by physical vapor deposition (PVD). The 2.2 nm HZO/1 nm ZrO_2/2.2 nm HZO stack is then grown consecutively by plasma enhanced atomic layer deposition (PEALD) at 250 °C without breaking the vacuum, wherein, $Hf[N(CH_3)_2]_4$, $Zr[N(CH_3)_2]_4$, and oxygen plasma are utilized as Hf, Zr, and oxygen sources, respectively. Additionally, a 5.4 nm conventional HZO film is also prepared for comparison. The Hf:Zr ratio is controlled by alternating the cycles of HfO_2 and ZrO_2. Subsequently, 50 nm W is sputtered on the FE film by PVD. After that, photolithography and etching are adopted to pattern and form the top electrode with an area of 80 × 80 μm^2. Finally, the capacitors are annealed at 400 and 450 °C in nitrogen atmosphere with rapid thermal annealing (RTA).

The microstructure and element analysis are performed by transmission electron microscopy (TEM), high-angle annular dark field (HAADF) measurement, and energy dispersion spectroscopy (EDS). The phase analysis is observed by grazing-incidence X-ray diffraction (GIXRD). The electrical characteristics are measured by a semiconductor analyzer (Agilent B1500A) and ferroelectric test system (Radiant Premier II).

3. RESULTS AND DISCUSSION

Figure 2a,b presents the cross-sectional TEM of the FE capacitor with an HZO/ZrO_2/HZO stack and conventional HZO annealed at 400 °C, respectively. The polycrystal nature of the FE stack is distinctly verified in the HZO/ZrO_2/HZO stack, and the insets demonstrate the (111) plane of the O-phase with a spacing of 2.92 Å in FE films annealed at 400 °C. However, the conventional HZO film exhibits an amorphous nature. Figure 2c shows the HAADF image of the FE capacitor with the HZO/ZrO_2/HZO stack and the EDS elemental distribution maps of all the elements. Figure 2d depicts the GIXRD results in the range of 25−35° in FE capacitors with the HZO/ZrO_2/HZO stack and conventional HZO film annealed at 400 °C. An obvious peak of the FE phase is observed around 30.4° in the HZO/ZrO_2/HZO stack, and the

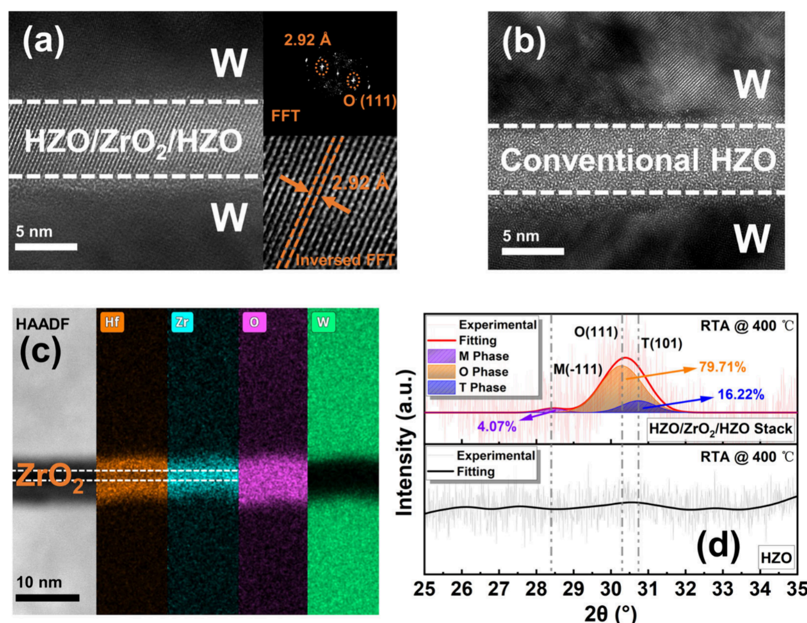


Figure 2. Cross-sectional TEM images of a capacitor with (a) an HZO/ZrO_2/HZO stack and (b) conventional HZO film annealed at 400 °C. The insets present the FFT and inversed FFT images of the O-phase. (c) The HAADF and EDS images for the distribution of Hf, Zr, O, and W elements in the capacitor with the HZO/ZrO_2/HZO stack annealed at 400 °C. (d) GIXRD results of capacitors with a HZO/ZrO_2/HZO stack and conventional HZO film annealed at 400 °C.

https://doi.org/10.1021/acsaelm.4c01745
ACS Appl. Electron. Mater. 2024, 6, 8507−8512

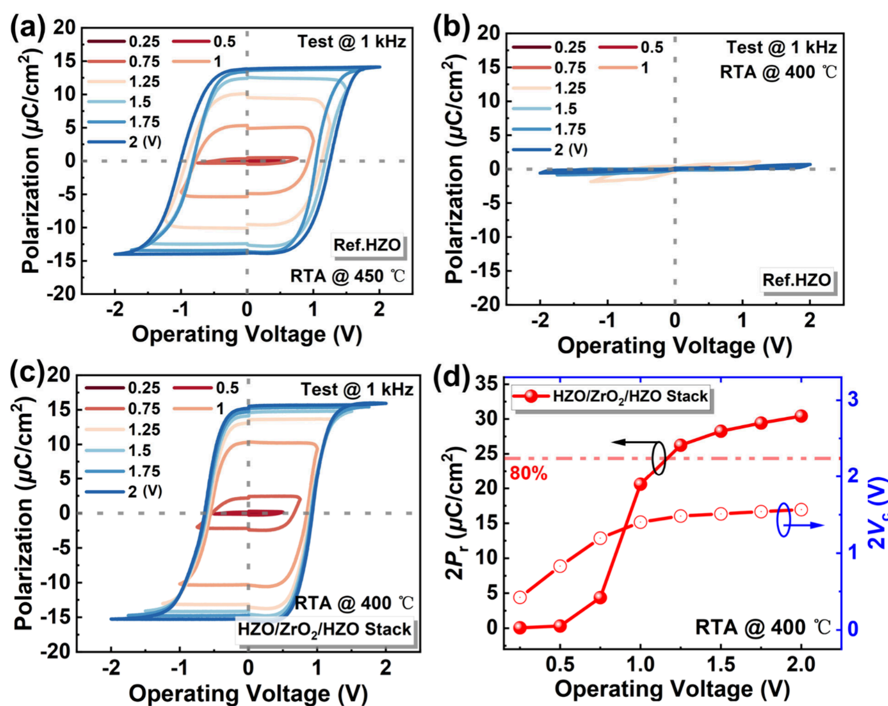


Figure 3. PUND measurements of FE capacitors with the conventional HZO film annealed at (a) 450 and (b) 400 °C under different operating voltages from 0.25 to 2 V. (c) PUND measurements of the capacitor with the HZO/ZrO_2/HZO stack under different operating voltages. (d) The extracted $2P_r$ and $2V_c$ as a function of operating voltage from the PUND measurement for the capacitor with the HZO/ZrO_2/HZO stack annealed at 400 °C.

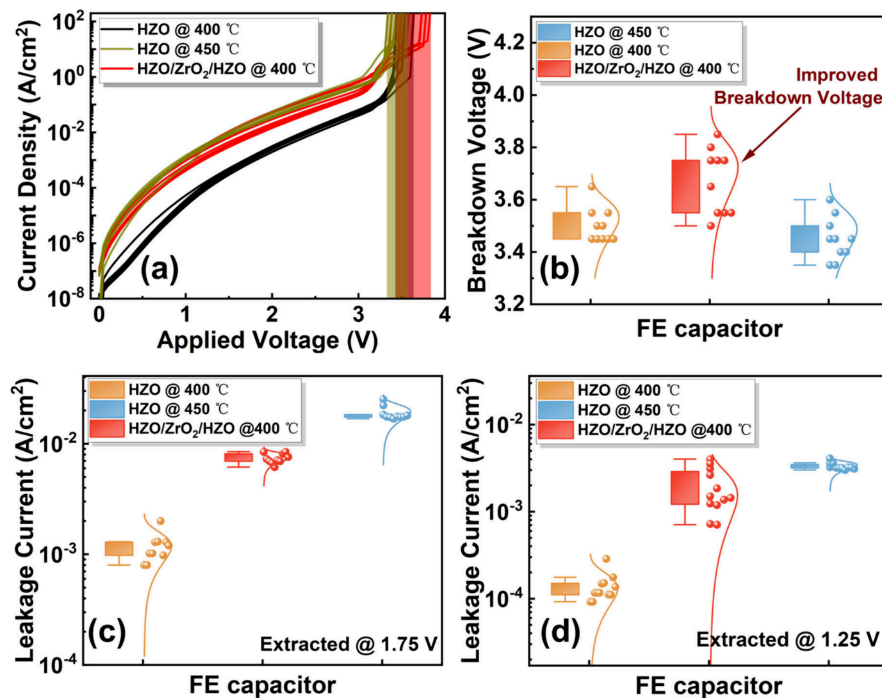


Figure 4. (a) TZDB characteristics of FE capacitors with conventional HZO film annealed in different temperatures and capacitors with the HZO/ZrO_2/HZO stack annealed at 400 °C. (b) Extracted breakdown voltages of fabricated capacitors. Note that the data were extracted from 10 samples for each annealing condition. The leakage current of FE capacitors extracted from the operating voltages of (c) 1.75 V and (d) 1.25 V.

proportions of the orthorhombic (O-) phase, tetragonal (T-), and monoclinic (M-) phases are 79.71, 16.22, and 4.07%, respectively, while the conventional HZO film displays a lack of crystallization. Such changes are mainly attributed to the tensile stress applied to the HZO films because of the coefficient of thermal expansion mismatch between the ZrO_2 and HZO film, which facilitates the crystallization of ultrathin ferroelectric film under low annealing temperature.[10,11]

Figure 3a,b illustrates the polarization−voltage (P−V) characteristics measured by positive-up-negative-down

https://doi.org/10.1021/acsaelm.4c01745
ACS Appl. Electron. Mater. 2024, 6, 8507−8512

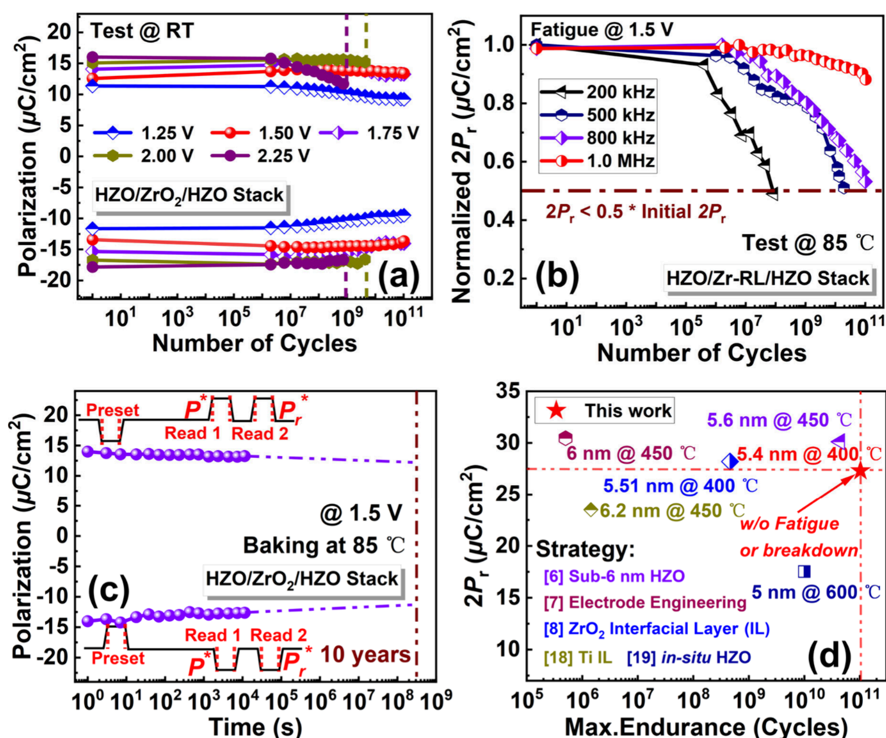


Figure 5. (a) The endurance characteristics of a capacitor with an HZO/ZrO_2/HZO stack annealed at 400 °C under different operating voltages from 1.25 to 2.25 V. (b) Cycling properties at 85 °C of the fabricated capacitor with the HZO/ZrO_2/HZO stack annealed at 400 °C under 1.5 V with different frequencies. (c) The retention time at 85 °C and pulse schemes of the FE capacitor with the HZO/ZrO_2/HZO stack annealed at 400 °C under 1.5 V. (d) Benchmark plot of polarization under maximum cycles and endurance.

(PUND) under different operating voltages from 0.25 to 2 V for an FE capacitor with the conventional HZO film annealed at 450 and 400 °C, respectively. As the annealing temperature decreases to 400 °C, the ferroelectricity disappears, which is ascribed to the significant phase formation barrier of thinner ferroelectric films that hinders the crystallization into the ferroelectric phase under a low annealing temperature below 400 °C.[5] In Figure 3c, $P-V$ curves of the FE capacitor with an HZO/ZrO_2/HZO stack annealed at 400 °C measured by PUND under different operating voltages from 0.25 to 2 V are presented. Complete $P-V$ curves and considerable $2P_r$ are obtained at operating voltages of 1 V and above. Figure 3d compares the $2P_r$ and $2V_c$ extracted from PUND measurements of the FE capacitor with the HZO/ZrO_2/HZO stack annealed at 400 °C under different operating voltages. Remarkably, the FE capacitor with a HZO/ZrO_2/HZO stack annealed at 400 °C achieves a $2P_r$ of 26.3 $\mu C/cm^2$ and a $2V_c$ of 1.48 V with a low operating voltage of 1.25 V.

Figure 4a,b displays the time-zero dielectric breakdown (TZDB) characteristics and extracted breakdown voltage (V_{BD}) of the fabricated capacitors, respectively. The capacitors with conventional HZO film annealed at 400 °C show the lowest leakage current, which is caused by its amorphous nature. Compared to the conventional HZO film annealed at 450 °C, the FE capacitors with the HZO/ZrO_2/HZO stack annealed at 400 °C exhibit reduced leakage current and improved breakdown voltage. This enhancement is primarily linked to the introduction of ZrO_2, which promotes the crystallization of the FE phase, lowers the annealing temperature, and thereby reduces the accumulation of thermal defects, which are mainly oxygen vacancies, during the annealing process.[12,13] Figure 4c,d shows the leakage current of the FE capacitor under 1.75 and 1.25 V, respectively. By the introduction of a ZrO_2 middle layer and the decrease of the annealing temperature, the leakage current of the FE capacitor is maintained at a low level while retaining its ferroelectricity. In contrast, the FE capacitor with conventional HZO films remains in an amorphous state at 400 °C, resulting in lower leakage current. However, the disappearance of ferroelectricity prevents their application in BEOL compatible memory systems. Therefore, HZO/ZrO_2/HZO stacked films effectively balance the ferroelectricity and dielectric leakage of the FE capacitor.

Figure 5a shows the endurance of the FE capacitor with an HZO/ZrO_2/HZO stack annealed at 400 °C under different voltages from 1.25 to 2.25 V at 1 MHz. It is observed that the capacitor breaks down at 4.37×10^9 and 7.33×10^8 when the operating voltages are 2 and 2.25 V, respectively. With the decrease of operating voltage, the FE capacitor with the HZO/ZrO_2/HZO stack demonstrates a stable $2P_r$ of 27.1 $\mu C/cm^2$ and superior cycling characteristics exceeding 10^{11} cycles without breakdown under the applied voltage of 1.5 V. To characterize the fatigue properties of the capacitor with the HZO/ZrO_2/HZO stack, the frequency-dependent behavior of the normalized $2P_r$ with cycling of the capacitor with the HZO/ZrO_2/HZO stack under 1.5 V at 85 °C was depicted in Figure 5b. Note that all capacitors underwent wake-up cycles at a frequency of 1 kHz before the fatigue test. The cyclic pulse utilizes a square wave with an amplitude of 1.5 V, and the read pulse employs the PUND measurements. The capacitor with the HZO/ZrO_2/HZO stack shows only ∼12% $2P_r$ degradation even after 10^{11} cycles under 1 MHz at 85 °C, and a half $2P_r$ loss ratio was obtained after 9.96×10^{10}, 1.93×10^{10}, and 8.64×10^7 cycles under 800, 500, and 200 kHz, respectively. The

https://doi.org/10.1021/acsaelm.4c01745
ACS Appl. Electron. Mater. 2024, 6, 8507−8512

excellent fatigue inhibition could be associated with the slow generation rate of new oxygen vacancies in the HZO/ZrO_2/HZO stack under low operating voltage, indicating less damage and domain pinning occurred in the thin films.[6,14−16] In addition, the retention time of the capacitor with the HZO/ZrO_2/HZO stack under 1.5 V after wake-up was further explored. The pulse schemes used for state retention measurements are illustrated in Figure 5c.[17] Stable polarization up to 10 years by linear extrapolation at 85 °C was obtained, as shown in Figure 5c. Figure 5d shows the benchmark plot of cycling characterization and $2P_r$ at maximum cycles of ultrathin HZO-based FE capacitors employing different strategies to optimize the endurance, as mentioned in previous reports.[6−8,18,19] In particular, the HZO/ZrO_2/HZO stack provides a more promising solution to decrease thermal budget and optimize the fatigue effect of FE capacitors while exhibiting excellent retention characteristics.

4. CONCLUSIONS

In summary, we have demonstrated a sub-6 nm HZO/ZrO_2/HZO stack prepared by ALD and the corresponding FE capacitors compatible with the BEOL process. The FE capacitors show a competitive $2P_r$ of 26.3 $\mu C/cm^2$ and V_c of 0.74 V under 1.25 V. Moreover, the capacitors with the HZO/ZrO_2/HZO stack achieve a highly stable $2P_r$ of 27.1 $\mu C/cm^2$ after 10^{11} cycles under 1.75 V without breakdown and only ~12% $2P_r$ degradation even after 10^{11} cycles under 1.5 V at 85 °C. These findings pave the way to engineering both the ferroelectricity and endurance for ultrathin FE devices compatible with BEOL process.

■ AUTHOR INFORMATION

Corresponding Author

Wenjun Liu − *School of Microelectronics, Fudan University, Shanghai 200433, P. R. China; Zhangjiang Fudan International Innovation Center, Fudan University, Shanghai 201203, P. R. China;* orcid.org/0000-0003-4217-8838; Email: wjliu@fudan.edu.cn

Authors

Yinchi Liu − *School of Microelectronics, Fudan University, Shanghai 200433, P. R. China*

Jining Yang − *School of Microelectronics, Fudan University, Shanghai 200433, P. R. China*

Hao Zhang − *School of Microelectronics, Fudan University, Shanghai 200433, P. R. China*

Dmitriy Anatolyevich Golosov − *Belarusian State University of Informatics and Radioelectronics, Minsk 220013, Belarus*

Chenjie Gu − *Department of Microelectronic Science and Engineering, School of Physical Science and Technology, Ningbo University, Ningbo 315211, P. R. China;* orcid.org/0000-0002-1339-4534

Xiaohan Wu − *School of Microelectronics, Fudan University, Shanghai 200433, P. R. China; Jiashan Fudan Institute, Fudan University, Jiaxing, Zhejiang 314100, P. R. China*

Hongliang Lu − *School of Microelectronics, Fudan University, Shanghai 200433, P. R. China;* orcid.org/0000-0003-2398-720X

Lin Chen − *School of Microelectronics, Fudan University, Shanghai 200433, P. R. China; Zhangjiang Fudan International Innovation Center, Fudan University, Shanghai 201203, P. R. China;* orcid.org/0000-0002-7145-7564

Shijin Ding − *School of Microelectronics, Fudan University, Shanghai 200433, P. R. China; Jiashan Fudan Institute, Fudan University, Jiaxing, Zhejiang 314100, P. R. China;* orcid.org/0000-0002-5766-089X

Complete contact information is available at: https://pubs.acs.org/10.1021/acsaelm.4c01745

Author Contributions

W. Liu initiated the project and coordinated the overall activities. Y. Liu was responsible for preparing the samples and conducting electrical testing and film characterization. J. Yang undertook the analysis of the mechanisms. All authors collaboratively discussed and interpreted the research findings and critically reviewed and revised the manuscript. All authors have endorsed the final version of the manuscript for publication.

Notes

The authors declare no competing financial interest.

■ ACKNOWLEDGMENTS

This work was supported by National Key Research and Development Program of China under Grant 2021YFB3202500 and Shanghai Municipal Science and Technology Commission under Grant 23511102300.

■ REFERENCES

(1) Schroeder, U.; Park, M. H.; Mikolajick, T.; Hwang, C. S. The fundamentals and applications of ferroelectric HfO_2. *Nature Reviews Materials* **2022**, *7* (8), 653−669.

(2) Park, M. H.; Lee, Y. H.; Kim, H. J.; Kim, Y. J.; Moon, T.; Kim, K. D.; Müller, J.; Kersch, A.; Schroeder, U.; Mikolajick, T.; et al. Ferroelectricity and Antiferroelectricity of Doped Thin HfO_2-Based Films. *Adv. Mater.* **2015**, *27* (11), 1811−1831.

(3) Lyu, X.; Si, M.; Capano, M. A.; Wang, H.; Ye, P. D. Ferroelectric and Anti-Ferroelectric Hafnium Zirconium Oxide Scaling Limit Switching Speed and Record High Polarization Density. *2019 Symposium on VLSI Technology* **2019**, T44−T45.

(4) Jiang, P.; Jiang, H.; Yang, Y.; Tai, L.; Gong, T.; Wang, Y.; Xu, P.; Lv, S.; Wang, B.; Gao, J.; Li, J.; Luo, J.; Yang, J.; Luo, Q.; Liu, M. A 256 Kbit $Hf_{0.5}Zr_{0.5}O_2$-based FeRAM Chip with Scaled Film Thickness (sub-8nm), Low Thermal Budget (350 °C), 100% Initial Chip Yield, Low Power Consumption (0.7 pJ/bit at 2V write voltage), and Prominent Endurance (>10^{12}). *2023 IEEE International Electron Devices Meeting (IEDM)* **2023**, 1−4.

(5) Park, J. Y.; Lee, D. H.; Park, G. H.; Lee, J.; Lee, Y.; Park, M. H. A perspective on the physical scaling down of hafnia-based ferroelectrics. *Nanotechnology* **2023**, *34* (20), 202001.

(6) Toprasertpong, K.; Tahara, K.; Hikosaka, Y.; Nakamura, K.; Saito, H.; Takenaka, M.; Takagi, S. Low Operating Voltage, Improved Breakdown Tolerance, and High Endurance in $Hf_{(0.5)}Zr_{(0.5)}O_{(2)}$ Ferroelectric Capacitors Achieved by Thickness Scaling Down to 4 nm for Embedded Ferroelectric Memory. *ACS Appl. Mater. Interfaces* **2022**, *14* (45), 51137−51148.

(7) Goh, Y.; Hwang, J.; Lee, Y.; Kim, M.; Jeon, S. Ultra-thin $Hf_{0.5}Zr_{0.5}O_2$ thin-film-based ferroelectric tunnel junction via stress induced crystallization. *Appl. Phys. Lett.* **2020**, *117* (24), 242901.

(8) Yu, E.; Lyu, X.; Si, M.; Ye, P. D.; Roy, K. Interfacial Layer Engineering in Sub-5-nm HZO: Enabling Low-Temperature Process, Low-Voltage Operation, and High Robustness. *IEEE Trans. Electron Devices* **2023**, *70* (6), 2962−2969.

(9) Liu, Y.-C.; Yang, J.-N.; Li, Y.-C.; Zhou, X.-L.; Xu, K.-L.; Chen, Y.-C.; Xie, G.-R.; Zhang, H.; Chen, L.; Ding, S.-J.; et al. Back-End of Line Compatible $Hf_{0.5}Zr_{0.5}O_2/ZrO_2/Hf_{0.5}Zr_{0.5}O_2$ Stack Achieving $2P_r$ of 39.6 $\mu C/cm^2$ and Endurance Exceeding 10^{10} Cycles Under Low-Voltage Operation. *IEEE Electron Device Lett.* **2024**, *45* (3), 388−391.

(10) Joh, H.; Jung, T.; Jeon, S. Stress Engineering as a Strategy to Achieve High Ferroelectricity in Thick Hafnia Using Interlayer. *IEEE Trans. Electron Devices* **2021**, *68* (5), 2538−2542.
(11) Liu, Y.-C.; Li, Y.-C.; Gu, Z.-Y.; Zhou, X.-L.; Huang, T.; Li, Z.-H.; Pi, T.-T.; Li, Y.-F.; Ding, S.-J.; Chen, L.; et al. Back-End of Line Compatible $Hf_{0.5}Zr_{0.5}O_2$ With ZrO_2 Seed Layer for Enhanced Ferroelectricity. *IEEE Electron Device Lett.* **2023**, *44* (7), 1116−1119.
(12) Huang, T.; Li, Y.-C.; Chen, C.-F.; Li, X.-X.; Gu, Z.-Y.; Zhang, D. W.; Zhu, X.-N.; Lu, H.-L. Demonstration of Robust Breakdown Reliability and Enhanced Endurance in Gallium Doped HfO_2 Ferroelectric Thin Films. *IEEE Electron Device Lett.* **2023**, *44* (9), 1476−1479.
(13) Lomenzo, P. D.; Takmeel, Q.; Moghaddam, S.; Nishida, T. Annealing behavior of ferroelectric Si-doped HfO_2 thin films. *Thin Solid Films* **2016**, *615*, 139−144.
(14) Xu, Y.; Yang, Y.; Zhao, S.; Gong, T.; Jiang, P.; Lv, S.; Yu, H.; Yuan, P.; Dang, Z.; Ding, Y.; et al. Robust Breakdown Reliability and Improved Endurance in $Hf_{0.5}Zr_{0.5}O_2$ Ferroelectric Using Grain Boundary Interruption. *IEEE Trans. Electron Devices* **2022**, *69* (1), 430−433.
(15) Kim, H. J.; Park, M. H.; Kim, Y. J.; Lee, Y. H.; Jeon, W.; Gwon, T.; Moon, T.; Kim, K. D.; Hwang, C. S. Grain size engineering for ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ films by an insertion of Al_2O_3 interlayer. *Appl. Phys. Lett.* **2014**, *105* (19), 192903.
(16) Pešić, M.; Fengler, F. P. G.; Larcher, L.; Padovani, A.; Schenk, T.; Grimley, E. D.; Sang, X.; LeBeau, J. M.; Slesazeck, S.; Schroeder, U.; Mikolajick, T. Physical Mechanisms behind the Field-Cycling Behavior of HfO_2-Based Ferroelectric Capacitors. *Adv. Funct. Mater.* **2016**, *26* (25), 4601−4612.
(17) Mueller, S.; Muller, J.; Schroeder, U.; Mikolajick, T. Reliability Characteristics of Ferroelectric Si:HfO_2 Thin Films for Memory Applications. *IEEE Transactions on Device and Materials Reliability* **2013**, *13* (1), 93−97.
(18) Segantini, G.; Barhoumi, R.; Manchon, B.; Cañero Infante, I.; Rojo Romeo, P.; Bugnet, M.; Baboux, N.; Nirantar, S.; Deleruyelle, D.; Sriram, S.; et al. Ferroelectricity Improvement in Ultra-Thin $Hf_{0.5}Zr_{0.5}O_2$ Capacitors by the Insertion of a Ti Interfacial Layer. *physica status solidi (RRL) - Rapid Research Letters* **2022**, *16* (10), 2100583.
(19) Liang, Y.-K.; Wu, J.-S.; Teng, C.-Y.; Ko, H.-L.; Luc, Q.-H.; Su, C.-J.; Chang, E.-Y.; Lin, C.-H. Demonstration of Highly Robust 5 nm $Hf_{0.5}Zr_{0.5}O_2$ Ultra-Thin Ferroelectric Capacitor by Improving Interface Quality. *IEEE Electron Device Lett.* **2021**, *42* (9), 1299−1302.