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# Back-end-of-line compatible $Hf_{0.5}Zr_{0.5}O_2$ ferroelectric devices enabled by microwave annealing

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**In this work, we demonstrate an extremely low annealing processing at 300 °C for the crystallization of $Hf_{0.5}Zr_{0.5}O_2$ (HZO) films with the adoption of microwave annealing (MWA). Compared to conventional annealing methods, an enhanced double remnant polarization ($2Pr$) of 55.4 μC/cm$^2$, a higher maximum dielectric constant, and nearly wakeup-free were realized by modulating the power of the microwave. It is believed that the increasing loss factor of zirconia with rising temperature allows more energy to be extracted from the microwave and transferred to the ferroelectric HZO molecules, which facilitates the crystallization at low temperature. Furthermore, an amorphous indium gallium zinc oxide ferroelectric field-effect transistor treated with microwave annealing was fabricated, and a competitive memory window of 1.5 V was substantially achieved. These findings offer insights into the integration of $HfO_2$ ferroelectric materials in non-volatile memory devices compatible with back-end-of-line (BEOL) in the future.**

**Keywords:** Microwave annealing, $Hf_{0.5}Zr_{0.5}O_2$, Ferroelectric capacitors, Remnant polarization, Back-end of line

## INTRODUCTION

Due to its compatibility with complementary metal-oxide-semiconductor technology and sub-10-nm scalability, the Zr-doped $HfO_2$ ($Hf_{0.5}Zr_{0.5}O_2$ [HZO]) ferroelectric (FE) device has garnered significant attention. It is considered as one of the most promising candidates for next-generation embedded non-volatile memories and logic devices[1–4]. With continuous innovations in internal computation, artificial intelligence, flexible synapses and machine learning, $HfO_2$-based FE devices compatible with BEOL process, including FE capacitors (FeCAPs), FE field-effect transistors (FeFETs), FE tunnel junctions, and FE random-access memory, have become focal points for future monolithic three-dimensional integration applications[5–8]. In the industry, high-temperature annealing processes have demonstrated significant usages, including the activation of ion implantation and the supplementation of nitrogen for TiN materials. Nonetheless, low-temperature annealing techniques for FE materials are essential in the BEOL process. The conventional annealing processes, including rapid thermal annealing (RTA) and furnace annealing (FA), which utilize a single mode of energy transfer, often result in the degradation of FE properties when the annealing temperature is reduced. This degradation poses significant challenges for the integration of FE devices[9–14].

For the integration of FE devices into memory systems compatible with the BEOL process, significant attempts have been made to fully balance the ferroelectricity and thermal budget. These efforts encompass interlayer engineering[15–19], electrode engineering[20–22], interface engineering[23], and modifications to the annealing process rooted in conventional processes[24]. Nonetheless, the non-ideal effects introduced by these methods, such as imprint and wakeup effects, continue to present substantial obstacles for the integration and application in the BEOL processes. Ultimately, this is primarily ascribed to the single energy transfer mechanism of conventional annealing processes, which necessitates additional design modifications in both structure and process to compensate for the performance degradation resulted from reduced annealing temperatures. Our previous work has reported high-performance amorphous indium gallium zinc oxide (α-IGZO) thin-film transistors processed at a minimal temperature of 189.6 °C via MWA[25]. In addition, Joh et al. presented a focus MWA method, which can effectively crystallize the HZO thin film into FE phase at a low process temperature[26]. Chen et al. investigated the FE HZO dielectric in metal-insulator-metal devices and metal-oxide-semiconductor capacitors by comparing the RTA and MWA[27]. All the aforementioned observations demonstrate that MWA shows significant advantages in device integration during BEOL processes. However, the impact of the process details of MWA on the performance of FE devices and non-ideal effects still requires further exploration.

In this work, an ultra-low crystallization temperature of approximately 300 °C was achieved by using MWA on the HZO film under the microwave power of 1400 W. Furthermore, a competitive 2*Pr* of 55.4 μC/cm$^2$, lower $E_c$ of 1.09 MV/cm, higher maximum dielectric constant and nearly wakeup free were demonstrated by modulating the power of annealing. In addition, an FeFET with a 10-nm α-IGZO channel annealing with MWA was fabricated, and an excellent MW of 1.5 V was obtained. The ultra-low crystallization temperature and high-quality FE properties provide an alternative approach for further memory devices compatible with BEOL.

## RESULTS AND DISCUSSIONS

Fig. 1a and b depict the process flow and schematic of the FeCAP, respectively. Fig. 1c shows the schematic diagram of the MWA process. In the MWA system, eight magnetrons were used as microwave sources, with a frequency of 5.8 GHz. To enhance the microwave absorption efficiency and improve the heating uniformity, quartz and silicon carbide wafers were typically placed inside the chamber as microwave susceptors. Prior to supplying the microwave power, a purge with 1200 s of $N_2$ gas was performed within the cavity to ensure the integrity of the gaseous environment inside.

Fig. 2a and b show the remnant polarization-voltage ($P$–$V$) and dynamic current-voltage ($I$–$V$) loops of the capacitor under 3.5-V sweeping with different microwave powers from 700 to 2800 W. The extracted $P_r$ and $E_c$ as a function of microwave power are presented in Fig. 2c. The capacitors annealed at 1400, 2100 and 2800 W exhibit the $2P_r$ of 26.8, 52.3 and 55.4 μC/cm$^2$, respectively. In addition, as the microwave power reached 2800 W, the $E_c$ of the FeCAP was continuously decreased to 1.09 MV/cm. This presents a significant advantage

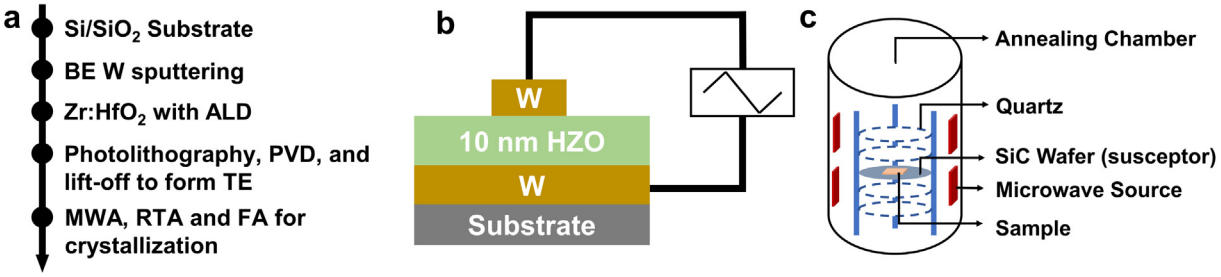


**Fig. 1 | Fabrication and schematic of the processes. a,** The process flow and **b,** schematic of FE capacitor. **c,** The schematic diagram of the microwave annealing process. Abbreviation: FE, ferroelectric.

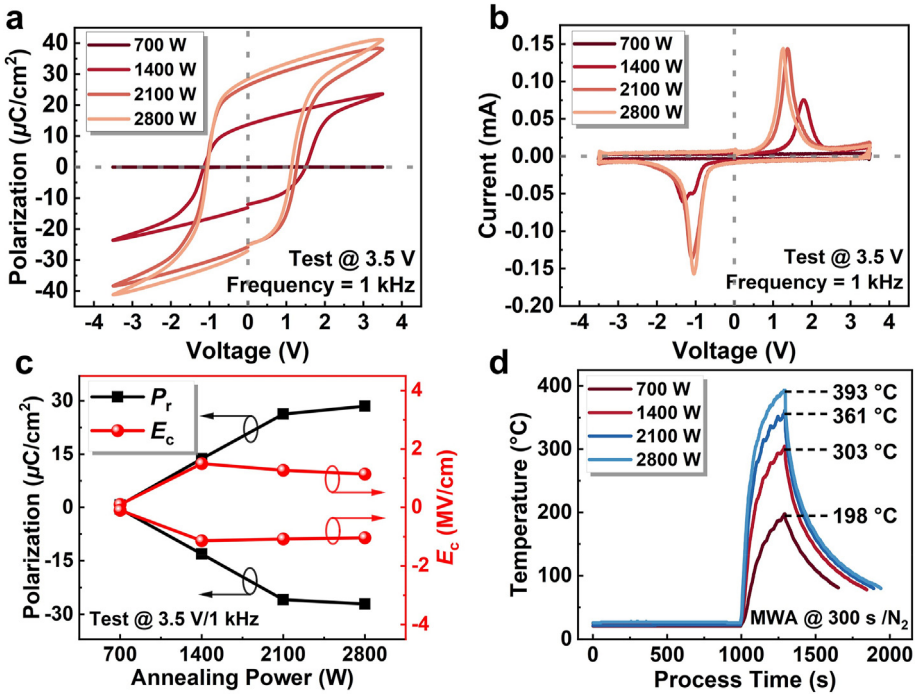


**Fig. 2 | Ferroelectricity of the capacitors annealed at MWA with different microwave powers. a,** $P$–$V$ and **b,** dynamic $I$–$V$ loops of capacitor with various annealing powers under 3.5 V at 1 kHz. **c,** The extracted $P_r$ and $E_c$ as a function of microwave power. **d,** Annealing temperature as a function of time for various MWA processes. Abbreviations: MWA, microwave annealing; $I$–$V$, dynamic current-voltage; $P$–$V$, polarization-voltage.

that distinguishes it from the existing literatures[18,23,24,28,29]. Fig. 2d shows the temperature as a function of time for various MWA powers, where the temperature is measured in real time with the adoption of an infrared pyrometer. MWA facilitates the development of ferroelectricity in the capacitor at the temperature of ~300 °C with the power of 1400 W, although the cavity temperature remains below 400 °C during the maximum power of MWA process up to 2800 W, which is fully compatible with the BEOL process. The reduced thermal budget is believed to be ascribed to the ability of MWA to directly transfer energy to the target material by vibration of polar molecules, which avoids excessive time and energy consumption during the annealing process. Additionally, during the process of microwave energy transfer, it will selectively couple with materials that exhibit higher dielectric losses, and the loss factor tends to increase with temperature, implying that HZO could absorb more energy for improved crystallization[25–27,30].

Fig. 3a–c present the $P$–$V$ curves obtained by the positive-up-negative-down test under the operating voltage ($V_{op}$) of 0.5 to 4.0 V. The extracted $2P_r$ and $2E_c$ as a function of $V_{op}$ for each annealing process are summarized in Fig. 3d. Comparative analysis shows that capacitors treated with MWA and RTA demonstrate enhanced $2P_r$ at low $V_{op}$ below 2.0 V, exhibiting a superior ferroelectricity in contrast to the capacitor treated with FA. Moreover, the capacitor treated with MWA shows a lower $2E_c$ than that treated with conventional annealing process. Fig. 3e shows the butterfly-shaped curves of dielectric constant-voltage ($\varepsilon$–$V$) for the capacitors treated with different annealing processes, indicating the existence of ferroelectricity[31–33]. The dielectric constants of the monoclinic phase (m-phase), orthorhombic phase (o-phase), and tetragonal phase (t-phase) of most $HfO_2$-based FE films are known to be ~17 to 20, 25 to 30, and 35 to 40, respectively[34]. It can be seen that the capacitor treated with MWA exhibits a higher dielectric constant than those annealed at RTA and FA, which primarily stems from the improved FE-phase ratio[18,35]. As shown in Fig. 3f, the diffraction peaks of the HZO films treated with MWA occur at a higher $2\theta$ angle than the those treated with RTA. Furthermore, the HZO films treated with RTA exhibit an additional diffraction peak around 31.8°, suggesting a more complex internal phase structure.

Fig. 4a–f show the $P$–$V$ loops under 2 to 3 V after wakeup cycling of capacitors treated with different annealing processes. Notably, the capacitors annealed with MWA and FA show their stability after applying 10 wakeup cycles. In contrast, the capacitor annealed at RTA shows a progressive increase in $P_r$ with continuous wakeup pulses application until reaching its stability after $10^4$ cycles. Under the high $V_{op}$ of 3 V, the capacitor treated with MWA exhibits a notably stable $P_r$ and $E_c$. Ten devices from each of annealing processes were randomly selected under uniform environmental conditions to determine their wakeup ratios and maximum $P_r$, which are summarized in Fig. 4g–i. The capacitor treated with MWA exhibits the lowest wakeup ratio among the above processes under 2 and 3 V sweeping. This enhancement could arise from the unique energy transmission in MWA, contributing to an improved phase structure within the HZO films and a more uniform distribution of oxygen vacancies than conventional annealing processes[36,37].

An FeFET with α-IGZO channel was subjected to MWA at the power of 2800 W for 300 s under $N_2$ atmosphere was prepared. To minimize the leakage current and optimize the interface between the α-IGZO channel and HZO thin film, a 2-nm aluminum oxide layer was introduced as an interfacial layer[38,39]. Fig. 5a and b show the key processes and schematic structure of the α-IGZO FeFET, respectively. Fig. 5c presents the cross-sectional transmission electron microscopy

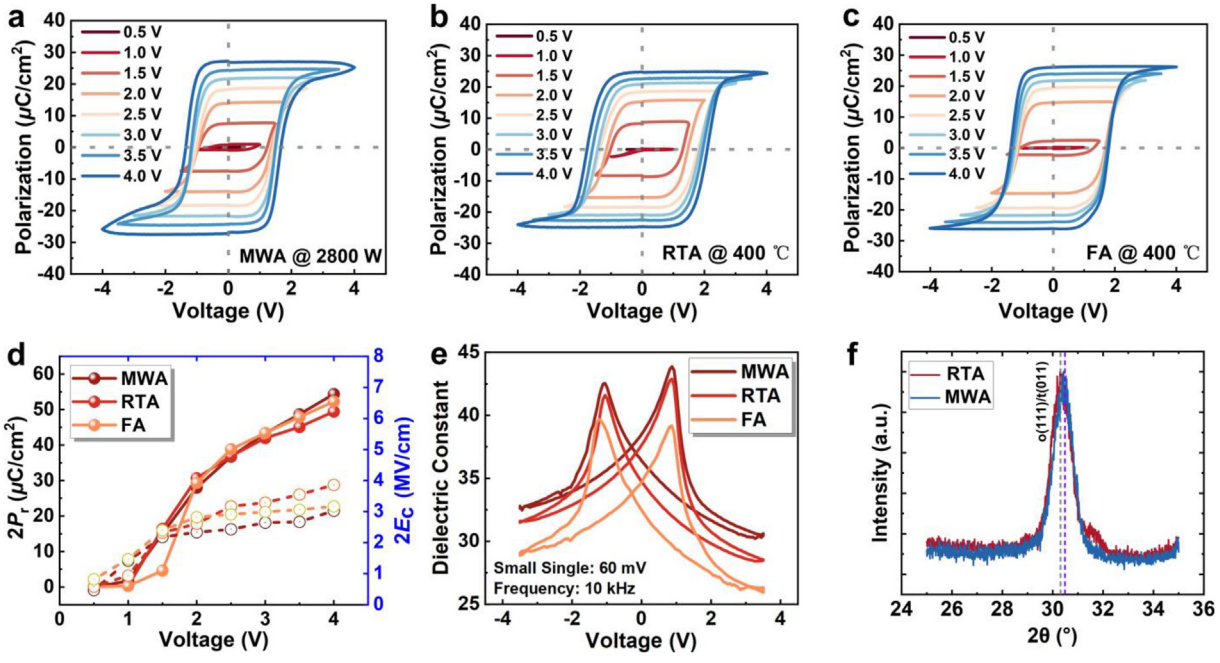


**Fig. 3 | The ferroelectricity of fabricated capacitors treated with different annealing processes.** The $P$–$V$ curves treated with **a,** MWA, **b,** RTA and **c,** FA under different $V_{op}$ from 0.5 to 4.0 V at 1 kHz. The extracted **d,** $2P_r$ and $2E_c$ as a function of $V_{op}$. **e,** Forward and reverse sweeps of dielectric constant-voltage between −3.5 and 3.5 MV/cm. **f,** The GIXRD results of the HZO films treated with RTA and MWA. Abbreviations: $P$–$V$, polarization-voltage; MWA, microwave annealing; RTA, rapid thermal annealing; FA, furnace annealing; *V*op, operating voltage; GIXRD, grazing-incidence X-ray diffraction; HZO, $Hf_{0.5}Zr_{0.5}O_2$.

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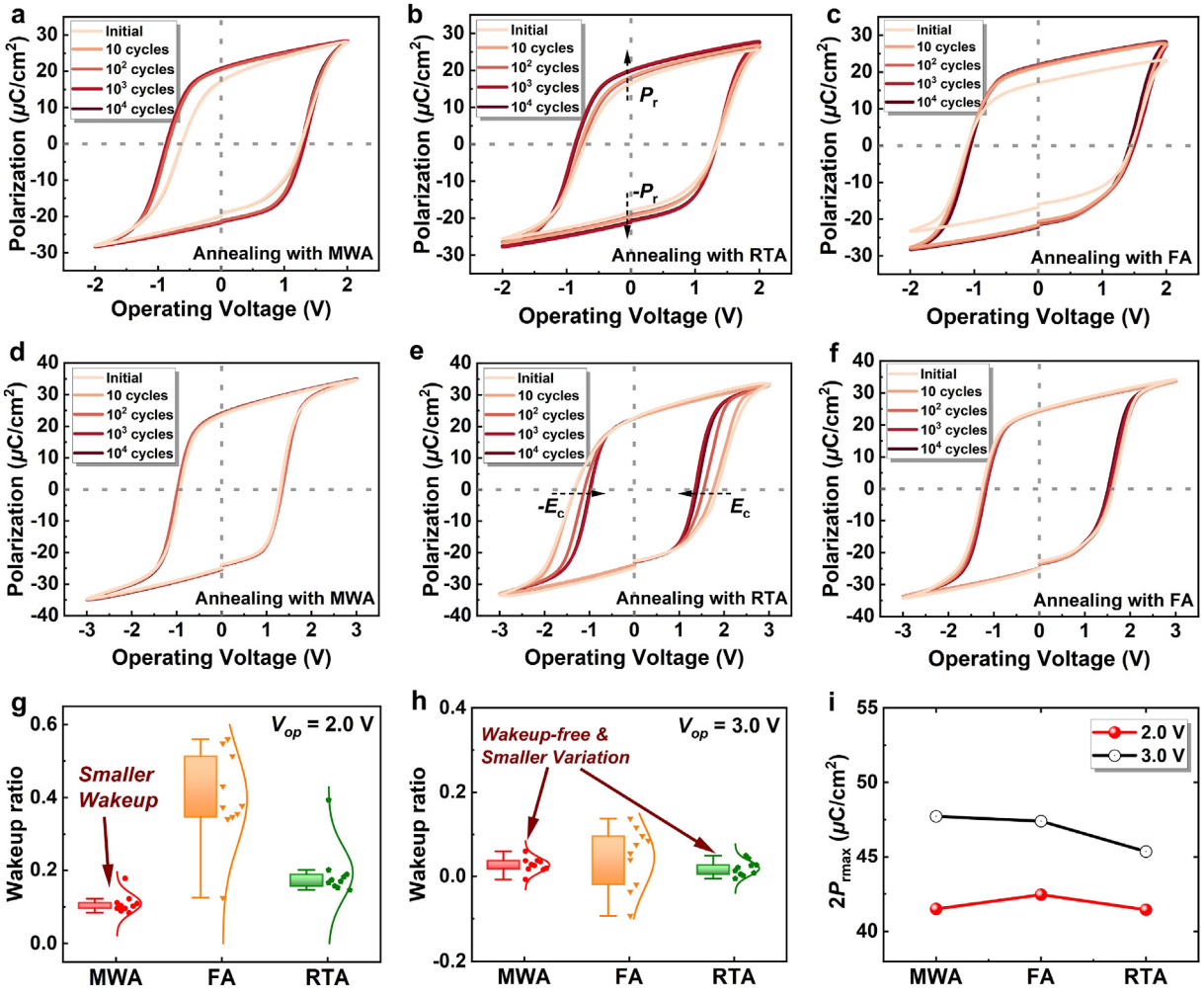


**Fig. 4 | The wakeup effect of the FE capacitors treated with different processes.** The $P-V$ loops under **a–c,** 2 V and **d–f,** 3-V sweeping after wakeup cycles. Extracted wakeup ratios ($1-P_{r\_initial}/P_{r\_max}$) under **g,** 2 V and **h,** 3-V sweeping. **i,** The extracted $2P_{r\_max}$ under different operating electric fields. Abbreviations: $P-V$, polarization-voltage; FE, ferroelectric.

(TEM) images of the α-IGZO FeFET structure. A clear and sharp interface between the channel and the FE layer guarantees its good interfacial property. Fig. 5d illustrates the high-angle annular dark field (HAADF) image of the fabricated α-IGZO FeFET and the energy dispersive X-ray spectroscopy (EDS) mapping diagrams of all the elements along the corresponding position. Fig. 5e shows the dual sweep $I_d$-$V_g$ curves of the α-IGZO FeFET with the gate voltage ranging from 1.0 to 3.5 V. It is noticeable that a threshold voltage ($V_{th}$) shift is observed under different gate voltages. This phenomenon is attributed to the accumulation of the positively charged oxygen vacancies, which are generated by the ionization of neutral oxygen vacancies within the semiconductor channel. These positively charged vacancies migrate and accumulate at the interface between the channel and the dielectric layer[25]. Once the gate voltage is removed, the need to maintain charge balance with the FE domains will cause the positively charged oxygen vacancies to become pinned at the interface.

On the other hand, the hydrogen donors introduced into the dielectric layer during the processes may migrate toward the channel under the influence of a negative gate voltage, ionizing to generate extra carriers and positive charges and leading to a threshold voltage shift[40]. A stable FE-type counterclockwise hysteresis is observed for the FeFET and the memroy window (MW) at a constant current of W/L × $10^{-7}$ A[41,42]. The extracted MW as a function of sweeping voltage is presented in Fig. 5f, showing that the maximum MW of 1.5 V is achieved under the sweeping voltage of 3.5-V. It is essentially close to its saturated MW even at 2.5 V. Fig. 5g depicts the output characteristics of the α-IGZO FeFET treated by MWA at 2800 W. With the increase in $V_{ds}$, the slope of the output curves also shows an increasing trend, suggesting the effective control ability of the gate voltage over the α-IGZO FeFET. Fig. 5h shows the output characteristics of the 10-nm α-IGZO FeFET in the linear region. Observations reveal the device's commendable linearity and saturation characteristics, highlighting a robust ohmic contact between the Cr/Au electrode and the α-IGZO channel layer.

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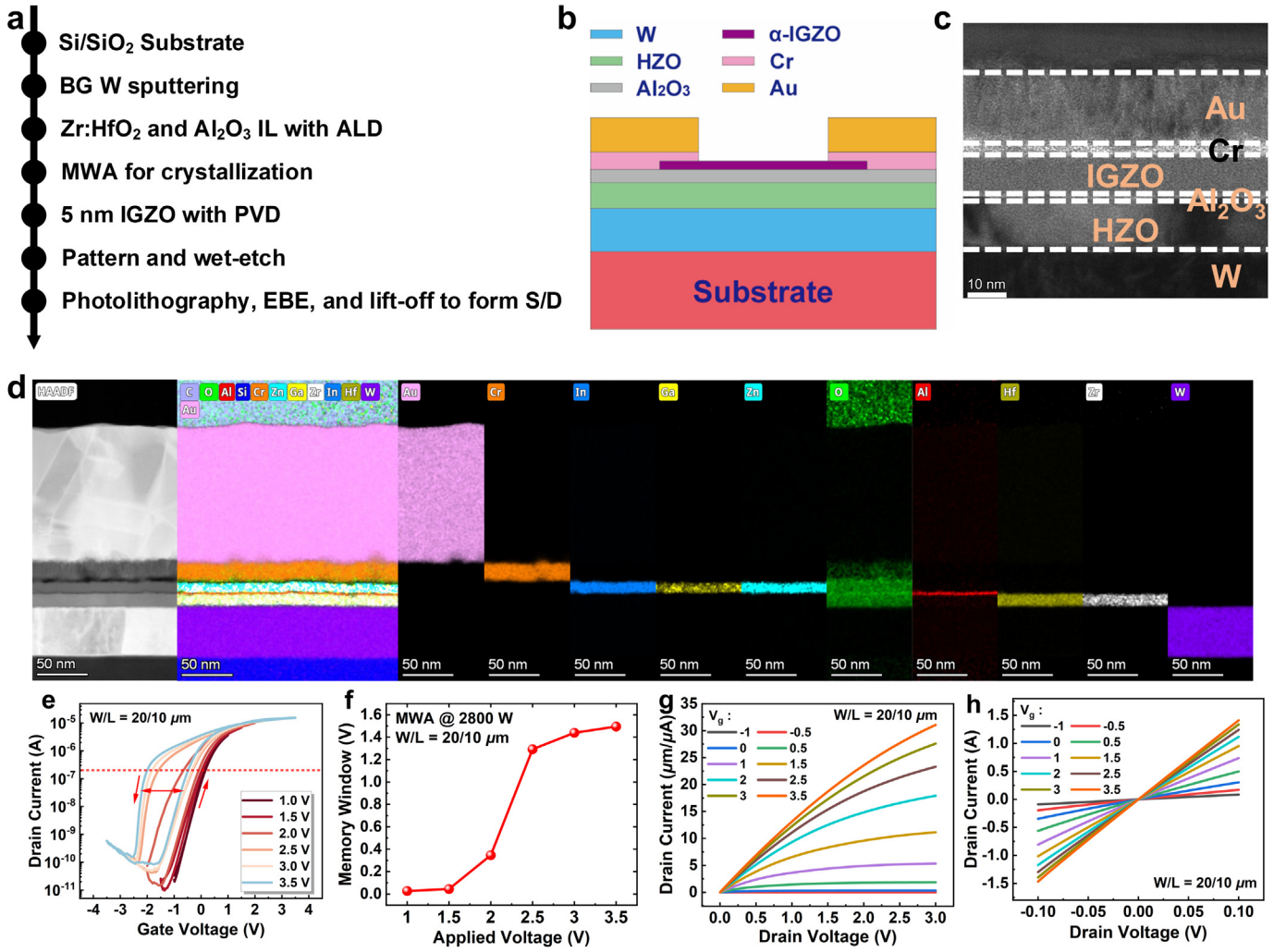


**Fig. 5 | The structure and electrical characteristics of the α-IGZO FeFET treated with MWA. a,** The process flow and **b,** the schematic structure of fabricated α-IGZO FeFET. **c,** Cross-sectional TEM and **d,** HAADF and EDS mapping images of the FeFET. **e,** Transfer characteristics under different gate voltages from 1.0 to 3.5 V with a fixed $V_{ds}$ of 100 mV. **f,** The extracted MW as a function of applied voltage. **g,** Output characteristics of the FeFET. **h,** The output characteristics in linear region. Abbreviations: α-IGZO, amorphous indium gallium zinc oxide; MWA, microwave annealing; FeFET, ferroelectric field-effect transistor; TEM, transmission electron microscopy; HAADF, high-angle annular dark field; EDS, energy dispersive X-ray spectroscopy; MW, memory window.

## CONCLUSION

In summary, we have achieved an ultra-low annealing temperature of approximately 300 °C with the adoption of the MWA process under 1400 W. Compared to conventional processes, a superior $2P_r$ of 55.4 μC/cm$^2$, lower $E_c$ of 1.09 MV/cm, and nearly wakeup free were demonstrated in the FeCAPs treated with MWA under 2800 W. Additionally, a considerable MW of 1.5 V was achieved in α-IGZO FeFETs. These findings suggest that the application of MWA is a feasible approach to optimize both the ferroelectricity and memory properties for FE device compatible with BEOL.

## METHODS

**Fabrication of the ferroelectric capacitor** Firstly, 30-nm tungsten (W) bottom electrodes were deposited onto the p-Si/$SiO_2$ (90 nm) substrate by physical vapor deposition (PVD). Next, the 10-nm HZO thin film was prepared by plasma-enhanced atomic layer deposition (PEALD) at 280 °C, using $Hf[N(CH_3)_2]_4$, $Zr[N(CH_3)_2]_4$, and oxygen plasma as the Hf, Zr, and oxygen sources, respectively. Afterwards, photolithography and PVD were used to pattern and sputter the 30-nm W top electrodes with an area of 100 × 100 μm$^2$. Finally, the FeCAPs with conventional HZO film were subjected to MWA under different microwave powers from 700 to 2800 W for 300 s under $N_2$ atmosphere, and the MWA process was performed using DGST-axom 200 at 5.8 GHz.

**Fabrication of the amorphous indium gallium zinc oxide ferroelectric field-effect transistor** Firstly, a 50-nm W bottom gate was grown by PVD at room temperature on a 90-nm $SiO_2$/P-Si substrate. Accordingly, a 15-nm HZO FE layer was prepared using PEALD at 280 °C. The deposited reactant precursors are consistent with the preparation of FeCAPs. Subsequently, a 2-nm $Al_2O_3$ layer was deposited onto the stack by thermal atomic layer deposition at 200 °C. $Al(CH_3)_3$ and $H_2O$ were chosen as aluminum and oxygen precursors.

Then, the device went through MWA at the power of 2800 W for 300 s under $N_2$ atmosphere for crystallization. After that, a 10 nm α-IGZO was deposited by PVD at room temperature, and the active channel layer was patterned by photolithography and wet etching (diluted HCl). The channel length and width are 10 and 20 μm, respectively. Finally, photolithography and electron beam evaporation were applied to pattern and form source and drain electrodes of Cr/Au (10/50 nm).

**Measurement of the fabricated devices** The microstructure and element analysis of the fabricated FeFETs were characterized by TEM (TalosF200XG2), HAADF, and EDS. The electrical performance was measured using a semiconductor device analyzer (Agilent B1500A) in a dark box at room temperature. The ferroelectricity of the devices was measured by FE test system (Precision Premier II).

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