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Special Topic: Novel Memory Materials and Devices: Ferroelectrics and Oxide Semiconductors

Enhanced memory window and reliability of α-IGZO FeFET enabled by atomic-layer-deposited HfO_2 interfacial layer

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Abstract The ferroelectric field-effect transistor (FeFET) with an amorphous indium–gallium–zinc oxide (α-IGZO) channel and an atomic-layer-deposited 2 nm HfO_2 interfacial layer (IL) was designed and fabricated to optimize both memory window (MW) and reliability. Compared with the FeFET without IL, the FeFET with 2 nm HfO_2 IL achieved an enhanced MW of 1.1 V at a reliable operating voltage with ultrafast current-voltage operation and an approximately 1000 times improvement in endurance with an available MW of ∼0.85 V after exerting pulses over 10^7 cycles while maintaining retention of over 10 years. This work proposes an effective strategy to enhance MW and reliability for future nonvolatile memory applications.

Keywords HfO_2, interfacial layer, $Hf_{0.5}Zr_{0.5}O_2$, memory window, reliability

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1 Introduction

Recently, ferroelectric field-effect transistors (FeFETs) based on metal oxide channel materials, such as amorphous indium–gallium–zinc oxide (α-IGZO) [1], indium oxide (In_2O_3) [2], and tungsten (W)-doped In_2O_3 [3], have been considered promising candidates for prospective applications in monolithic 3D integration toward large-scale memory, motivated in part by the low power consumption, high writing speed, complementary metal–oxide–semiconductor technology compatibility, and outstanding scalability of HfO_2-based FeFET [4–6]. However, the application of FeFETs is still restricted by their narrow memory window (MW) and poor endurance, which are not only associated with the ferroelectric (FE) layer itself but also linked to the interface between the channel and the gate insulator [7]. Significant efforts and progress have been made to optimize the memory properties of FeFETs, such as interfacial layer (IL) thickness reduction via oxygen scavenging in Si-based FeFET [8] and IL-free gate stacks in α-IGZO FeFET [9]. However, a large gate voltage drop across the low-k IL and an inferior MW in the IL-free gate structure are unexpectedly obtained. The memory performance of FeFETs was improved by introducing Al_2O_3 IL [7] and Al_2O_3/ZrO_2 stack IL [10]. By inserting Al_2O_3 IL and scaling down the In_2O_3 channel length, Lin et al. [2] obtained and reported an optimized MW, which is measured by the ultrafast current-voltage (UFIV) operation. Comparatively, the combination of the metal sacrificial layer and high-k IL in oxide FeFET could be an effective method for device property enhancement [11]. In this work, α-IGZO FeFETs with a 2 nm HfO_2 IL were constructed. The fabricated FeFET with HfO_2 IL exhibited a competitive MW of ∼1.1 V and enhanced program and erase speeds. Subsequently, excellent reliability with continuous loading over 10^7 cycles and extrapolated retention of >10 years were achieved.

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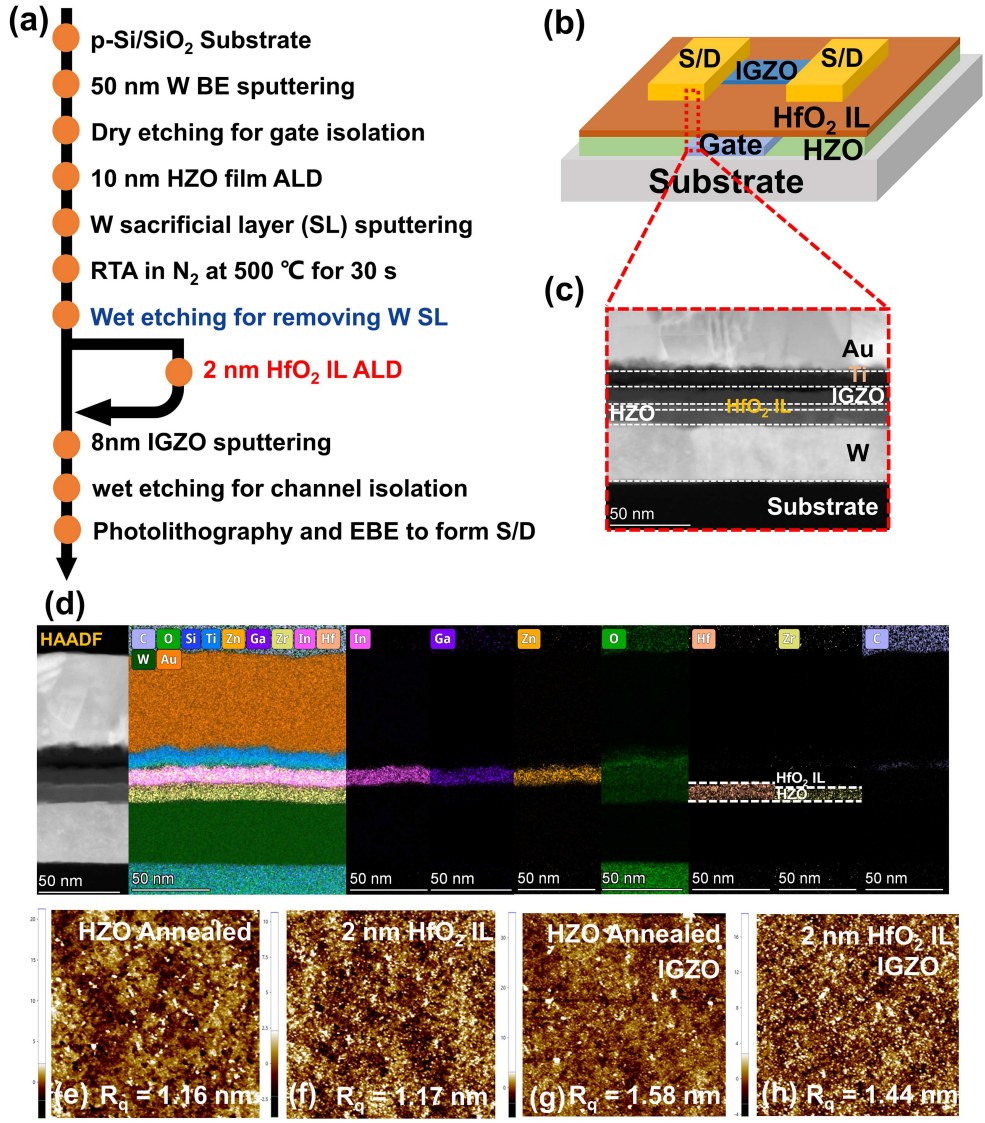

Figure 1 (Color online) (a) Process flow, (b) schematic, (c) cross-sectional TEM, and (d) HAADF and EDS mapping images of the fabricated FeFET with 2 nm HfO_2 IL. The distribution mapping of the elements In, Ga, Zn, O, Hf, Zr, and C is presented below. AFM images of (e) annealed HZO film, (f) HfO_2 IL, (g) IGZO on annealed HZO, and (h) IGZO on HfO_2 IL with the scanning size of 5 μm × 5 μm.

2 Device fabrication

The process flows of the fabrication of FeFETs with and without HfO_2 IL are shown in Figure 1(a). First, a 50 nm W thin film was deposited onto the SiO_2/p-Si substrate using physical vapor deposition, followed by photolithography and SF_6/CHF_3 inductively coupled plasma dry etching for gate isolation. Next, 12 nm $Hf_{0.5}Zr_{0.5}O_2$ (HZO) was prepared by atomic layer deposition (ALD) at 280°C with $Hf[N(CH_3)_2]_4$, $Zr[N(CH_3)_2]_4$, and O_2 as Hf, Zr, and oxygen precursors, respectively. The W was then deposited on the thin film as the capping layer because it effectively induces HZO crystallization [12]. Thereafter, the thin films went through rapid thermal annealing at 500°C for 30 s in N_2 atmosphere for crystallization, and the W capping layer was removed by wet etching with H_2O_2:H_2O = 1:2 and a trace amount of NH_4OH. Afterward, 2 nm HfO_2 was grown by ALD at 250°C as IL, and a control device without HfO_2 IL was also prepared. Subsequently, 8 nm α-IGZO was constructed by radio frequency magnetron sputtering at room temperature, and the active channel layer was patterned by photolithography and wet etching (diluted HCl). Finally, photolithography and electron beam evaporation were adopted to pattern and form the source and drain contacts of Ti (10 nm)/Au (50 nm). The surface roughness of the FE dielectric layer and semiconductor channel layer was measured using atomic force microscopy (AFM). The microstructure

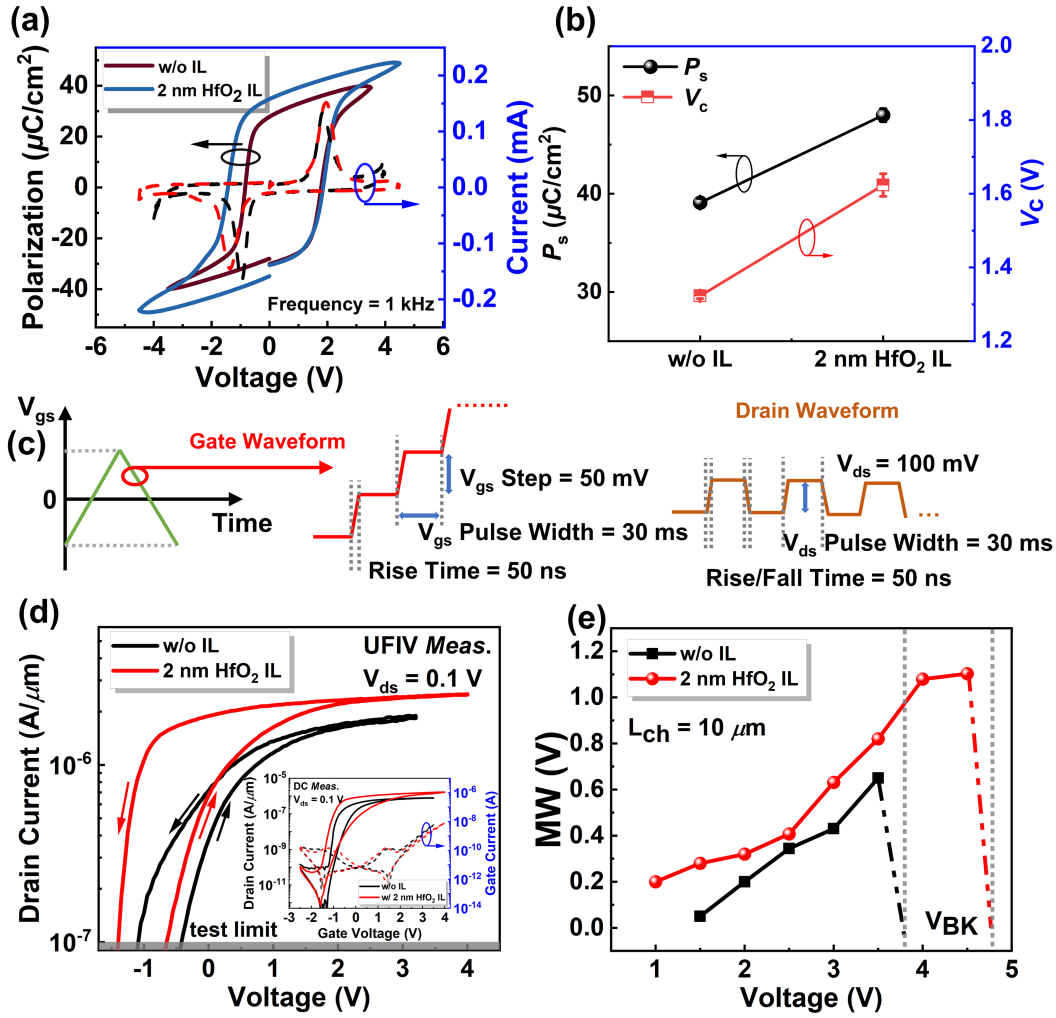

Figure 2 (Color online) (a) P-V and dynamic I-V loops of the FE capacitor based on the MFIM structure without and with 2 nm HfO_2 IL under a reliable operating voltage. (b) P_s and V_c of the MFIM structure. (c) Schematic of the UFIV measurements. (d) I_d-V_g of α-IGZOFeFETs with different gate stacks under the UFIV test method. The I_d-V_g and I_g-V_g curves of the FeFETs based on the DC measurements are shown in the inset in (d) as basic information. (e) MW of α-IGZO FeFETs without and with 2 nm HfO_2 IL at V_{ds} of 0.1 V.

and element analyses of the fabricated FeFETs were characterized by transmission electron microscopy (TEM), high-angle annular dark field (HAADF), and energy-dispersive X-ray spectroscopy (EDS). The electrical performance was measured using a semiconductor device analyzer (Agilent B1500A). The ferroelectricity of the devices was measured using a field-effect test system (Precision Premier II).

3 Results and discussion

Figure 1(b) shows the schematic view of the FeFET. Two different FeFET structures were fabricated. One sample without IL was designed as the control device, and the other sample with 2 nm HfO_2 IL was used as the experimental device. Figure 1(c) presents the cross-sectional high-resolution TEM images of the FeFET with HfO_2 IL, confirming its clear structure and good interfacial property. Figure 1(d) depicts the HAADF image of the FeFET and the EDS distribution mapping diagrams of all of the elements, showing the distributed elements In, Ga, Zn, O, Hf, Zr, and C in the fabricated FeFET. Notably, the FeFET with HfO_2 IL exhibits sharp interfaces both structurally and chemically without obvious interdiffusion. In addition, the difference in the position and thickness of the elements Hf and Zr verifies the presence of 2 nm HfO_2 IL. Figures 1(e)–(h) show the AFM images of annealed HZO film, HfO_2 IL, IGZO on annealed HZO, and IGZO on HfO_2 IL, where the surface roughness values were 1.16, 1.17, 1.58, and 1.44 nm, respectively.

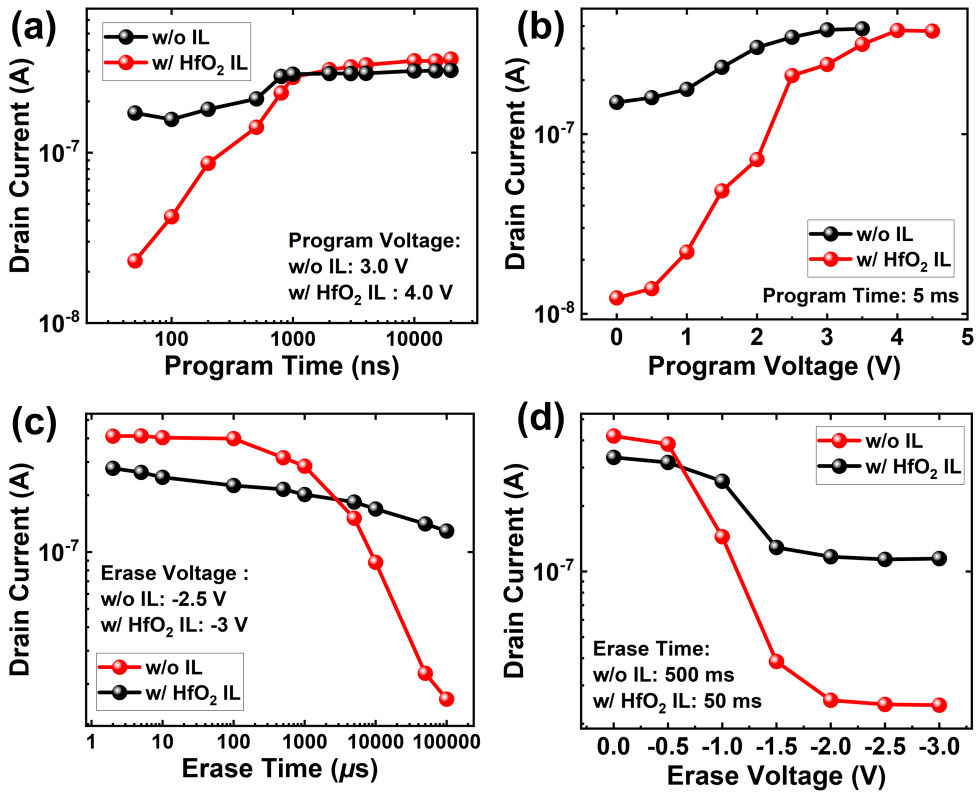

Figure 3 (Color online) Dependence of I_d on the (a) program time, (b) program voltage, (c) erase time, and (d) erase voltage of FeFETs with and without HfO_2 IL.

Figure 2(a) displays the polarization-voltage (P-V) and dynamic current-voltage (I-V) characteristics at reliable voltage ranges of FE capacitors without and with 2 nm HfO_2 IL. Compared with the control device, larger spontaneous polarization (P_s) and coercive voltage (V_c) were observed in the capacitor with HfO_2 IL, as shown in Figure 2(b). Although the HfO_2 IL could induce undesired voltage distribution, it substantially increases the reliable voltage range and enhances P_s under a higher operating voltage ($V_{\rm op}$). Notably, large P_s and V_c values could improve the memory properties of FeFET [11,13]. Accordingly, the MW of the FeFETs was measured using the UFIV method, which is reported to suppress charge trapping during voltage sweep [2,7]. Figure 2(c) presents the detailed waveforms and parameters obtained from the UFIV operation. The measurement step and pulse width of gate voltage (V_g) are 50 mV and 30 ms, respectively. Similarly, the drain voltage (V_d) is applied with an amplitude of 100 mV and a pulse width of 30 ms. Figure 2 shows the I_d-V_g curves obtained from the UFIV measurements at V_d = 0.1 V for FeFETs with and without HfO_2 IL. The inset in Figure 2(d) shows the I_d-V_g and I_g-V_g curves obtained from the DC measurements. A stable FE-type counterclockwise hysteresis is observed for all FeFETs, with MW up to 1.1 V by integrating 2 nm HfO_2 IL. These results reflect a positive correlation between the MW of FeFET and P_s and $2V_c$, which is consistent with previous reports [2,7]. Furthermore, the DC measurements shown in the inset in Figure 2(d) reveal similar MW enhancement and negative differential-resistance-type behavior in the I_d-V_g and I_g-V_g curves [14]. Here, the FeFETs with and without HfO_2 IL show comparable on-state current of $\sim 10^{-6}$ A, and the decrease in the on-state current in the FeFET without HfO_2 IL could be associated with its increased surface roughness [15]. Figure 2(e) depicts the MW of the FeFETs as a function of the operating voltage, showing that the incorporation of HfO_2 IL resulted in an enhanced MW and increased breakdown voltage. The improved MW is primarily attributed to the optimization of the electric-field distribution within the gate stack and the effective suppression of electron trapping through the utilization of HfO_2 IL [16].

Furthermore, the cumulative programming and erasing characteristics of FeFETs with and without HfO_2 IL were explored by applying V_g pulses with incremental amplitudes or widths. Following each V_g pulse, I_d was measured at a V_d of 0.1 V and a V_g of 0 V. As the program time and voltage increase, the FE domains progressively switch from the erased state to the programmed state, as shown in Figures 3(a)

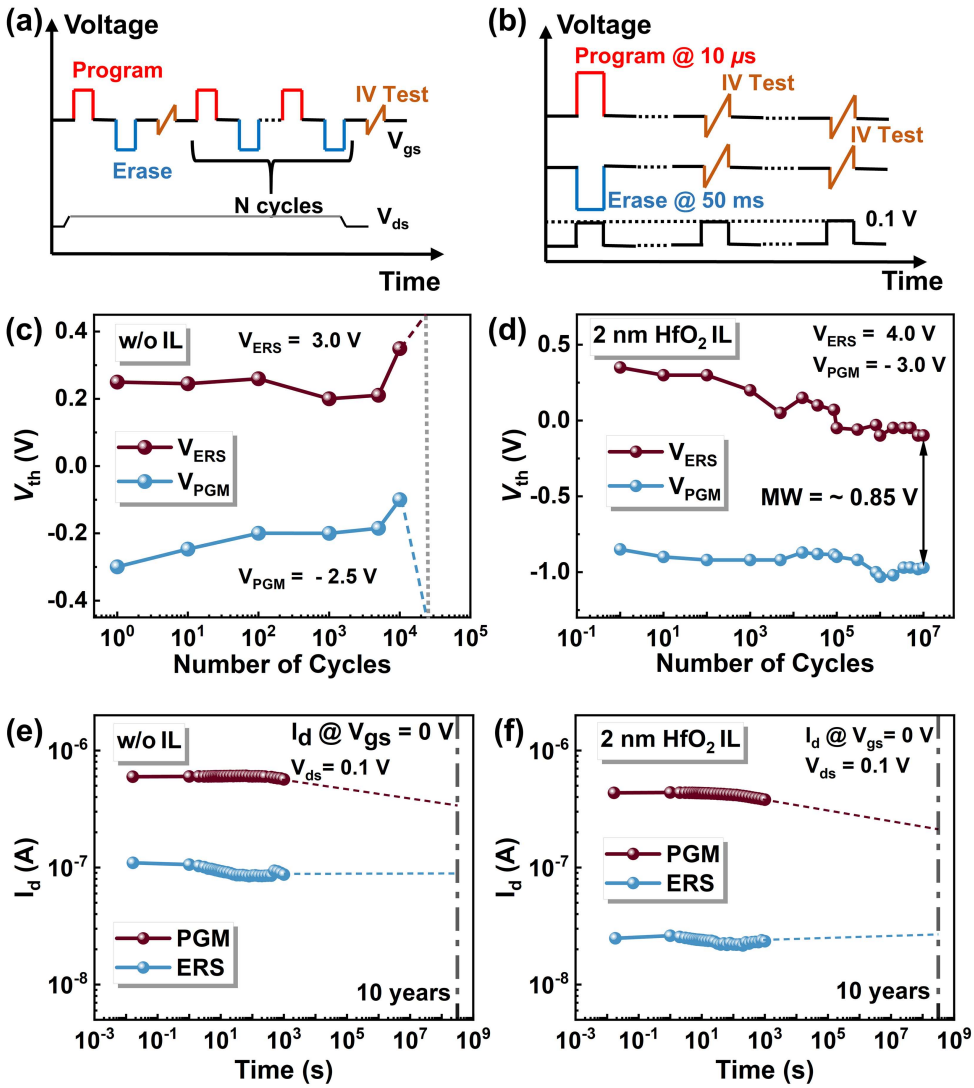

Figure 4 (Color online) Pulse sequence for (a) endurance and (b) retention testing used. Evolution of $V_{\rm th}$ with program and erase cycling for the device (c) without and (d) with HfO_2 IL. Retention characterization of the device (e) without and (f) with HfO_2 IL.

and (b). By contrast, as the erase voltage or pulse width increases, the FE domains begin to switch from the programmed to the erased state, leading to a reduction in I_d. Compared with the FeFET without IL, the FeFET with 2 nm HfO_2 IL exhibits an enhanced current MW and shorter program and erase times. Notably, the erasing speed is significantly slower than the programming speed, which is mainly related to the n-type oxide semiconductor that hardly generates holes under the external electric field. As a result, the accumulation of holes at the channel/insulator interface could not occur rapidly, directly hindering the effective electric field on the FE layer [17,18].

To further examine the influence of HfO_2 IL on the memory properties of α-IGZO FeFET, the endurance and retention characteristics of FeFETs without and with HfO_2 IL were measured and analyzed. The pulse sequence for reliability and retention testing used is shown in Figures 4(a) and (b), respectively. The pulse widths of the program and erase processes are 10 μs and 50 ms to ensure complete programming and erasing. Figures 4(c) and (d) display the cycling characteristics of FeFET by loading fatigue cycles. Compared with the control device, the FeFET with HfO_2 IL shows better reliability, lighter degradation of MW, and even no breakdown until an endurance of $\sim 10^7$ cycles. The enhanced reliability is believed to be associated with the improved cycles-to-breakdown, resulting from the suppression of defect generation during cycling due to the insertion of HfO_2 IL [19]. Figures 4(e) and (f) present the retention characterization of the FeFETs. Notably, the FeFETs exhibit a stable I_d after programming

and erasing, and the retention of >10 years is obtained by linear extrapolation.

4 Conclusion

In summary, we have designed and fabricated an α-IGZO FeFET with atomic-layer-deposited HfO_2 IL with enhanced MW and reliability. By integrating 2 nm HfO_2 IL between α-IGZOand HZO dielectrics, a larger MW of ∼1.1 V is achieved compared with the FeFET without IL. Moreover, a superior MW of ∼0.85 V is still maintained after the endurance of $\sim 10^7$ cycles, and the extrapolated retention of >10 years is projected. These findings provide an alternative method to boost the MW and reliability of FeFETs via interfacial engineering.

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