Manuscript Click here to view linked References

Performance analysis of TSV and MEMS capacitive sensor integration based on COMSOL

Chenxi Yue [a], Jiabo Zhao [a], Linxi Dong [a*], Jiagen Cheng [a], Uladzimir Fiadosenka [a,b], Gennady Gorokh [b], Jianhao Zhang [a], Chaoran Liu [a], Weihuang Yang [a], Zengfeng Di [c]

[a] College of Electronics and Information, Hangzhou Dianzi University, Hangzhou 310018, China

[b] R&D Laboratory of Nanotechnologies, Belarusian State University of Informatics and Radioelectronics, 220013 Minsk, Belarus

[c] Shanghai Institute of Microsystem and Information Technology, Chinese Academy of Sciences, Shanghai 200050, China

ARTICLEINFO

Keywords:
Integration
Through-silicon-via
Performance analysis
COMSOL
Reliability

ABSTRACT

At present, the integration technology of through-silicon vias (TSVs) and micro-electro-mechanical systems (MEMS) has reached a certain level of development, which can address the issue of area cost of the entire system, but the impact on the performance of the two integrations is not too much discussion. Since the parasitic effect of TSV may affect some aspects of the performance of MEMS sensors, this paper analyzes the integrated performance of TSV and MEMS capacitive sensors through theoretical derivation and finite element method (FEM) of COMSOL simulation. Firstly, the derivation and simulation verification of TSV parasitic parameters and variation trends are made, and a suitable TSV model and MEMS capacitive sensor model are obtained. Secondly, theoretical derivation is made on the influence of the parasitic effect on the system output and the impact of the excitation signal on the system reliability. Finally, the simulation of the integrated model by COMSOL verifies the trend consistency of the theoretical results. This article confirms that TSV parasitic effects affect sensors of different sizes to varying degrees. A through hole with a diameter of 10μm (aspect ratio 2:1) can increase the sensitivity of a small cavity model by up to 2.63% (19.96fF/N). Additionally, it improves the stable equilibrium range and recovery rate of the system.

* Corresponding authors.

E-mail addresses: donglinxi@hdu.edu.cn (L. Dong).

1. Introduction

MEMS has a wide range of applications across numerous fields of modern society. The advantages of MEMS, including their small size and low cost, have contributed to a gradual increase in demand, particularly in recent years with the advent of artificial intelligence (AI) and the robot concept industry, which have introduced heightened requirements for the volume and performance of sensing modules [1]. Usually, MEMS achieve demand-side performance optimization through structural innovation. However, it is unrealistic to expand the new structure while maintaining other indicators. This is particularly prominent in terms of volume requirements. Moreover, most MEMS must be combined with integrated circuits (IC) for use in an electronic system, which makes the space requirements of the entire system more demanding [2,3].

In recent decades, two-dimensional integration has been the main way for MEMS-IC integration [4,5]. The modules are deployed in a planar manner, making the system relatively large. Until the emergence of 3D stacked structures [4,6], the use of space is further optimized. However, 3D stacking uses wire bonding, which has problems with transmission and reliability. With the emergence of chip-level packaging and wafer-level packaging concepts, a more compact 3D packaging model [7] has been derived, and its area only depends on the maximum chip area. This concept requires vertical through-holes, usually silicon Through-hole (TSV) has the advantage of shorter signal paths, improved system reliability and smaller parasitic effects [8]. After the birth of this concept, many researchers and companies [7]-[10] have carried out the integrated design of MEMS-ASIC, proposed many bonding modes and process flows, and laid the foundation for the integration of MEMS-TSV-ASIC mode.

The existing TSV process is already very mature, and similar integrated products are also available in the market [11], but its cost has increased exponentially. It is still unknown whether the performance of the final product can be stably complemented by the additional cost. This article aims to study the impact of TSV structure on MEMS performance. In this work, due to the complexity and specificity of ASIC, there are various results in the qualitative analysis of the module. Therefore, MEMS capacitive sensors are used to implement TSV bonding in the model, and the variation of TSV performance under different parameters and the effect of TSV bonding on the performance of MEMS capacitive sensors are investigated to provide some guidance for the comprehensive consideration of system performance and cost.

2. Simulation Model and Theoretical Basis

2.1. TSV Basic Parameter Analysis

Common TSV structures include cuboid, cylindrical, conical (truncated cone) and ring-cylindrical structures [12]. There are also new structures derived from the above basic structures such as coaxial ring columns cylinders and carbon nanotube-filled structures. In actual production, the existing process level and performance impact should be comprehensively considered for structural design. There are two types of capacitances through silicon vias, one is dielectric layer parasitic capacitance, and the other is silicon substrate capacitance (C_{sub}) [13]. Due to the different materials between the contact surfaces, the parasitic capacitance of the dielectric layer of the through silicon hole can be refined into two parts. One part is the oxide layer (insulating layer) capacitance formed by the contact between the insulating layer silicon dioxide and different materials on both sides (C_{ox}), and the other part is the depletion layer capacitance (C_{dep}) formed near the silicon substrate depending on the operating voltage. Fig. 1 shows the basic parameters of TSV and the location of parasitic capacitance (without depletion layer), where D is called the TSV center distance, r_a and r_b are the two bottom radius of the TSV respectively, h is the depth of the TSV, α is the inclination angle of the conical through silicon hole, t is the thickness of the oxide layer (insulating layer) silicon dioxide.

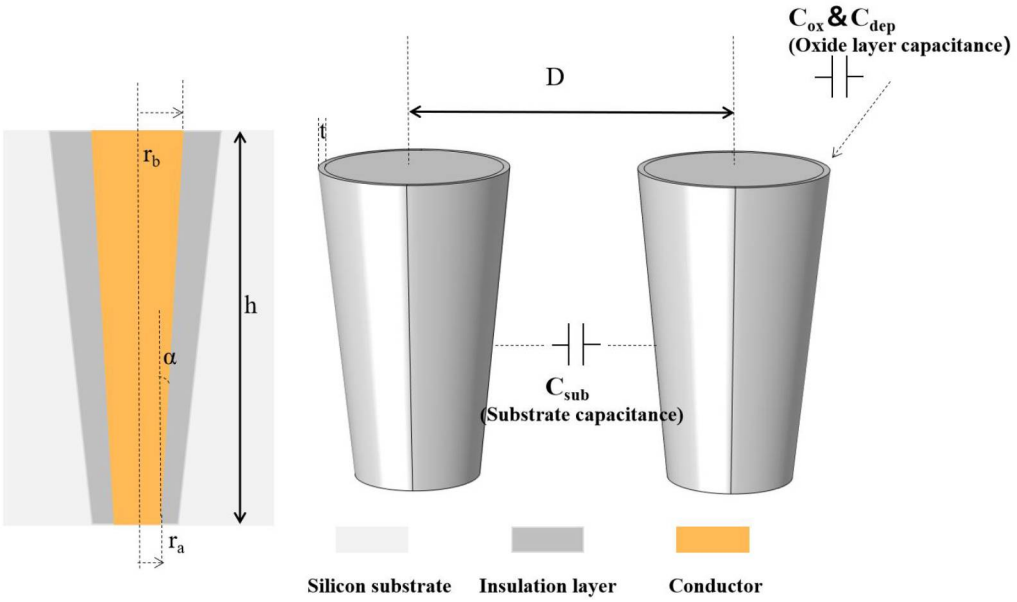


Fig. 1. Schematic diagram of basic parameters of TSV.

The theoretical capacitance calculation formula can be derived from the following equation [14]:

$$C_{ox}=\frac{Q}{U}=\frac{2\pi h\varepsilon_{sio2}}{\cos\alpha\ln\left[\frac{2(r_\alpha+t_{ox})+h\beta^T}{2r_\alpha+h\beta^T}\right]} \quad (1)$$

$$C_{dep}=\frac{Q}{U_{dep}}=\frac{2\pi h\varepsilon_{si}}{\cos\alpha\ln\left[\frac{2(r_\alpha+t_{ox})+h\beta^T}{2(r_\alpha+t_{ox}+t_{dep})+h\beta^T}\right]} \quad (2)$$

$$C_{sub}=\frac{2\pi D\varepsilon_{si}}{\cos\alpha\ln\left(2r_a+D\beta^T\right)} \quad (3)$$

Where $\beta^T=\tan\alpha$, Q represents the amount of charge on the closed surface, ε_{sio_2} is the relative permittivity of the insulating silicon dioxide.

By calculating the above formula in MATLAB, preliminary conclusions can be drawn:

(1) The depth of TSV is positively correlated with the parasitic capacitance of the insulation layer.

(2) The thickness of the insulation layer is inversely related to the parasitic capacitance of the insulation layer.

(3) The center-to-center spacing between TSVs is inversely related to the parasitic capacitance of the substrate.

The simulation of TSV shape and basic parameters uses COMSOL solid mechanics and steady-state research of electrostatic fields. Table I shows the parameters of the simulated materials.

Table 1.

Material Parameters Used in The Model

Material	Density(kg/m3)	Relative permittivity	Poisson's ratio	Young's modulus (GPa)
Si	2330	11.7	0.06	170
SiO2	2200	3.9	0.30	70
BCB	1000	2.6	0.34	3
Cu	8960	1.0	0.35	110

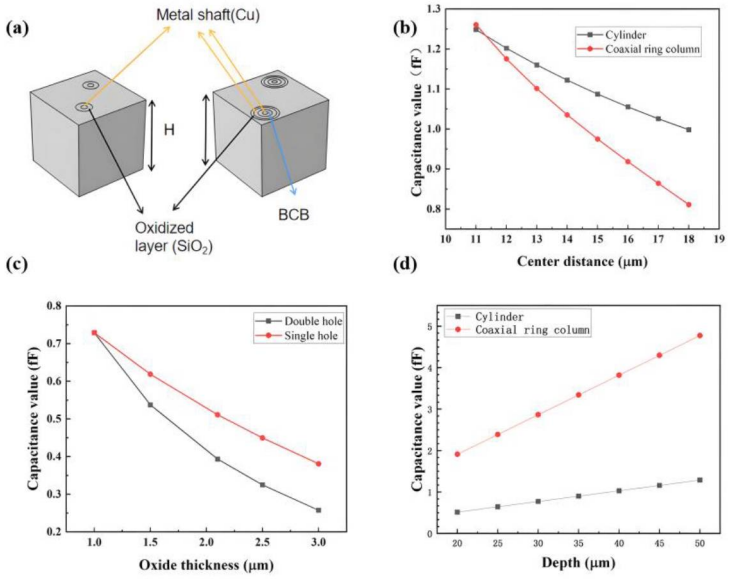
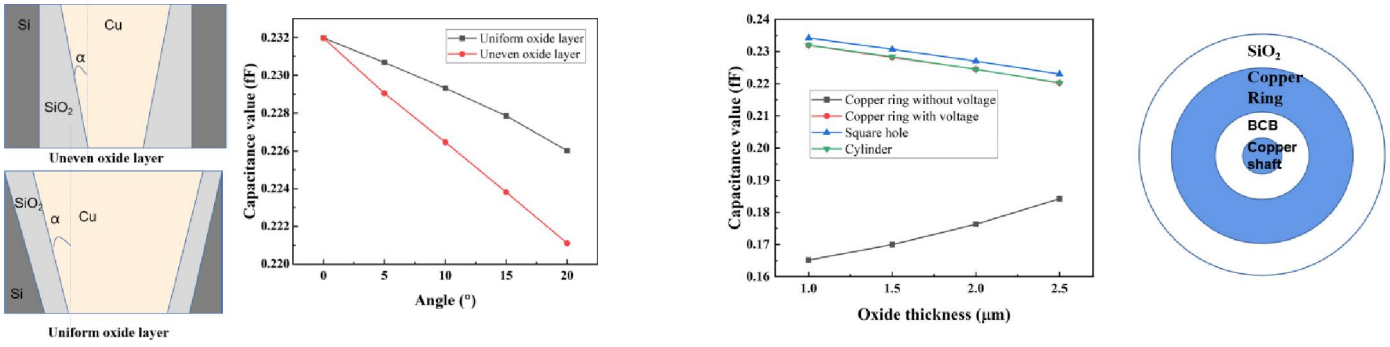


Fig. 2. Comparison of cylindrical and coaxial ring columns (a) model structure. (b) relationship between center distance and global capacitance. (c) relationship between cylindrical TSV single and double hole oxide layer thickness and global capacitance. (d) relationship between depth and global capacitance.

In Fig. 2, the voltages of two TSV metal shafts with the same size are 0V and 1V respectively, which are used as signal lines and ground lines. The maximum radius of TSV is 5μm. When comparing cylinders and coaxial ring columns, keep the model at 50μm×50μm×H (depth) in a silicon substrate, and BCB is filled between the ring-column metal layers as buffer and insulation, and the remaining parameters remain consistent.

In the simulation results shown in Fig. 2, the parameter trend changes are consistent with the theoretical part. It should be emphasized that Fig. 2b and Fig. 2d are diagrams showing the relationship between the center spacing and the via depth of the two structures on the capacitance. Due to the complexity of the material, the initial parasitic capacitance of a coaxial ring column of the same size is usually higher than that of a cylinder. At the same time, the accumulation rate of the parasitic capacitance of a coaxial ring column in depth (0.09548fF/μm) is 3.7 times that of a cylinder (0.0257fF/μm). However, due to the shielding characteristics of the coaxial ring-column structure [15], the drop rate of the parasitic capacitance at the center spacing (0.0642fF/μm) is 2.02 times that of the cylinder (0.03178fF/μm). Generally, coaxial ring pillars gain advantages in transmission and thermodynamics through high parasitic capacitance and process difficulty [16], while basic cylindrical TSV sacrifices part of the transmission performance and stability through low parasitic capacitance and simple process. Fig. 2c refers to whether the thickness of the oxide layer of the two through holes changes consistently when there are two TSVs at the same time. When the double holes change uniformly, the rate of decrease of the parasitic capacitance in the thickness of the oxide layer (0.2356fF/μm) is 1.35 times that of the single hole (0.1741fF/μm).



(a) (b)

Fig. 3. (a) Relationship between different tilt mode angles and global capacitance. (b) The effect of oxide layer thickness on the global capacitance under different conditions and the schematic diagram of the ring structure.

The bottom of the cylindrical via the hole in the TSV process may have an inclination angle. Currently, the model appears as a conical or frustoconical shape, and the shape of the oxide layer has a certain impact on the parasitic capacitance. Fig. 3a shows the relationship between downhill and parasitic capacitance for different oxide layer models. The influence of the tilt angle of the uneven oxide layer model is 1.82 times that of the uniform oxide layer model. This means that non-ideal factors in the processing process have a greater impact.

Since the copper ring in the coaxial ring column may be separated from the electrostatic field in the selection of device functions, the copper ring is partially excluded from the electrostatic field in the simulation and the sum of the thickness of the oxide layer and the copper ring is a constant value. At this time, the change of the oxide layer will have an opposite trend (Fig. 3b), and this function and the size of the oxide layer of the TSV in the normal mode should be considered comprehensively. To reduce complexity, interference factors, and process difficulty, a relatively simple cylindrical TSV was selected for the TSV layer in the MEMS-TSV system model to explore the performance impact.

2.2. *MEMS Capacitive Sensor Model*

The simplest capacitor can be formed by two metal plates, its basic formula is expressed as:

$$C=\frac{\varepsilon S}{4k\pi d} \tag{4}$$

where ε is the relative permittivity, S is the facing area between the plates, k is the electrostatic force constant, and d is the distance between the plates.

To obtain the impact of TSV on MEMS capacitive sensors more intuitively, the MEMS device part should not be overly complicated. The model used in the study mainly consists of a silicon substrate (including the top mass), a metal plate, a cavity, and a TSV layer. The TSV layer and the bottom metal plate are bonded through BCB. The TSV diameter is 10μm (aspect ratio 2:1) to ensure that it is smaller than the minimum size of the bottom metal plate. The silicon beam thickness is 25μm, the metal plate thickness is 5μm, the cavity thickness is 10μm, the overall size of the MEMS part is 1000μm×1000μm×115μm, and the TSV layer size is 1000μm×1000μm ×20μm (Fig. 4a-d).

The sensitivity of the MEMS component can be enhanced by establishing parallel connections between the plates, as illustrated in Fig. 4e [17]. However, the three-layer plate is difficult to implement in terms of technology and requires additional openings in the silicon matrix when bonding with TSV. To amplify the sensitivity of the sensor part and the change after bonding TSV, the model uses a smaller cavity, but it will have a certain impact on the range and edge effects.

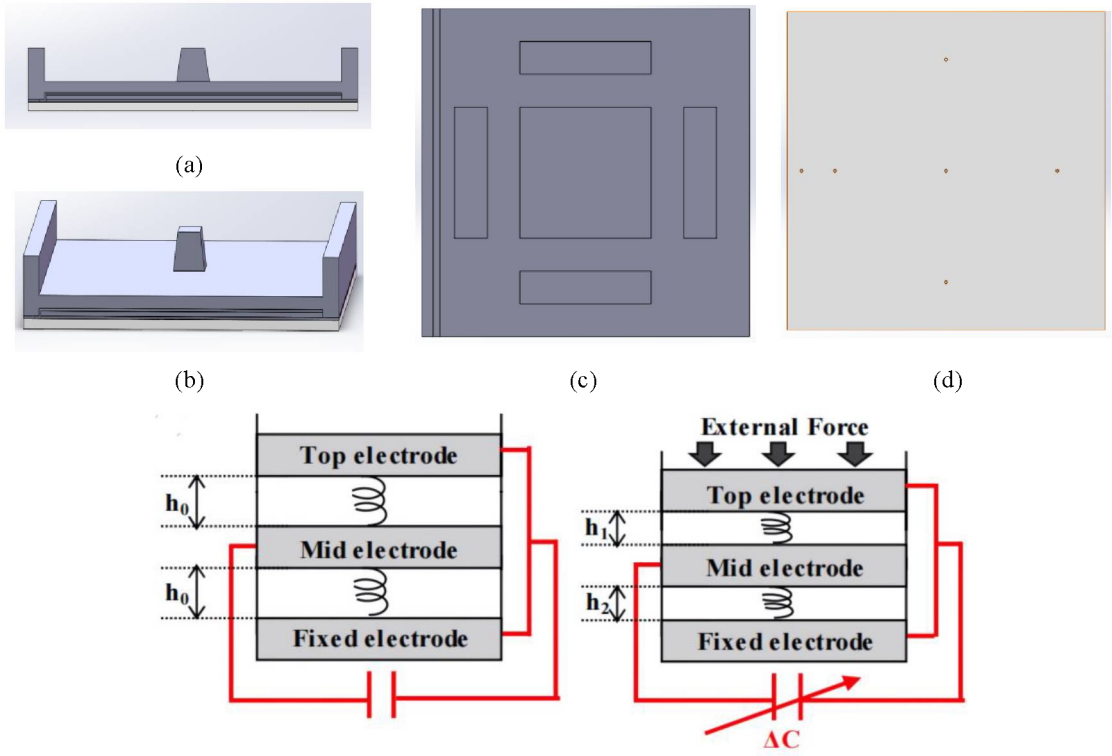


Fig. 4. (a) Front view of MEMS capacitive sensor model. (b) Stereo view of MEMS capacitive sensor model. (c) The bottom plate of the MEMS capacitive sensor model. (d) TSV layer through hole location. (e) Principle of parallel connection of plates to improve sensitivity.

2.3. Integrated Analysis of MEMS-TSV

(1) The relationship between metal plate signal mode and output

Under normal circumstances, a metal plate of the capacitive sensor is connected to the system as a ground signal line, but there are also special cases. For example, in the multi-metal plate coaxial ring column, the output signal of this model can be selected according to the function of the plate combination output. At this time, the parasitic capacitance brought by TSV will be different from the usual situation.

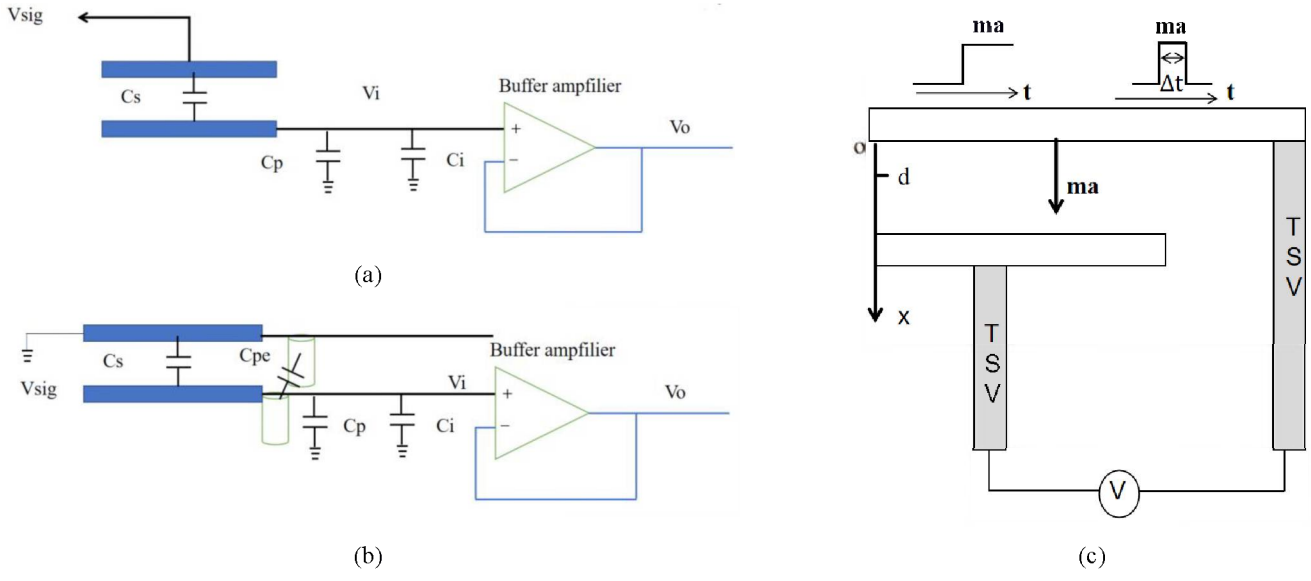


Fig. 5. (a) Ungrounded plate output mode. (b) Grounded plate output mode. (c) TSV system and stimulus input.

Fig. 5a shows the capacitance distribution and output when two signal lines are used as output. Among them, *Vsig* and *Vi* are the voltage signals of the two plates, *Cs* is the capacitance between the plates, *Cp* is the TSV parasitic capacitance, and *Ci* is the parasitic capacitance introduced by the system input. In this mode, the output is determined by the following formula:

$$\left(V_{sig}-V_i\right)C_s\omega-V_i\left(C_p+C_i\right)\omega=0 \tag{5}$$

$$V_o=V_i=\frac{V_{sig}C_s}{\left(C_s+C_p+C_i\right)} \tag{6}$$

Referring to (2), the linearity of the output has nothing to do with the signal frequency. When the TSV size is determined, the linearity of the output only depends on the capacitance change between the plates, and eventually becomes stable.

When there is a ground wire connected to the system in the signal line, the output mode is shown in Fig. 5b, where *Cpe* is part of the parasitic capacitance introduced by the TSV and connected in parallel to the plate. The output currently is:

$$V_o=V_i=\frac{V_{sig}C_{sp}}{\left(C_{sp}+C_p+C_i\right)} \tag{7}$$

Among them *Csp*=*Cs*+*Cpe*. This equation shows that *Cpe* also determines the linearity change of the output, especially when affected by edge effects.

(2) The relationship between metal plate signal mode and output

Since the capacitance of MEMS capacitors is usually small, stray capacitance and parasitic capacitance have a great influence on their performance. The existence of TSV will introduce this part of capacitance, which will lead to changes in the reliability of the system and have a certain impact on the response of the excitation signal.

Fig. 5c shows a simplified capacitor system with TSV. It can be demonstrated that the pull-in voltage in the absence of an external force is [18,19]:

$$V_{po}=\sqrt{\frac{8kd^3}{27S\varepsilon\varepsilon_0}} \tag{8}$$

Where ε_0 is the vacuum dielectric constant and *d* is the plate spacing. The above formulas only consider the situation when there is capacitance between the plates. When the TSV is bonded to the plates, the above formulas need to be corrected. After bonding can be divided into two situations:

(i)The capacitance of the series part can be proportionally equivalent to the expanded spacing *Δd* of the capacitor plates, and this equivalent value is related to the thickness of SiO2 at the bonding point. The equivalent spacing is replaced by *d* in (6). The series part will increase the upper limit of the pull-in voltage, which also means that the parasitic capacitance introduced by the series part will expand the stable point balance distance. When this value is three times the distance between the plates, the pull-in effect will no longer occur. When the system size is reasonable, the capacitance of the series part is negligible, and the stability change can be disregarded. However, series capacitance can be used as a method to eliminate the pull-in effect at large voltages that cause device reliability problems.

(ii)Substrate parallel connection refers to the section of the silicon substrate where the parasitic capacitance of two or more TSVs is connected to the plate signal line. This configuration is analogous to the grounded plate output mode. Parasitic capacitance enters the plates in parallel to change the amount of the charge stored. The formula is simplified with dimensionless symbols, $\gamma=b\rho$ 、 $\rho=\frac{x}{d}$ and $b=\frac{C_p}{\left(C_p+C_0\right)}$ are recorded and combined with the equilibrium conditions to obtain:

$$\gamma(1-\gamma)^2=\frac{S\varepsilon\varepsilon_0 V^2 b}{2kd^3} \tag{9}$$

This means that when the parasitic capacitance $C_p \le 0.5C_0(\gamma=\frac{1}{3})$, there will be no pull-in effect, and the magnitude of the parasitic capacitance is almost in line with this range. The balance range may be expanded by connecting a capacitor $C \ge 0.5C_0$ in parallel, although this will result in a maximum pull-in voltage.

Therefore, TSV improves the stability of the system under electrostatic force but is limited by the relative sizes of TSV and capacitive sensors. The balance of parasitic effects in frequency characteristics and stability must be comprehensively considered in device design.

When a force excitation signal is introduced, the stability situation will change accordingly.

When the upper plate connected to the mass block is subjected to the step inertia force *ma* at the equilibrium position x_0, the maximum displacement equation of the mass block is as follows:

$$q(\overline{x_m})=\frac{1}{2}\left(\overline{x_m}+\overline{x_0}\right)-\frac{p}{\left(1-\overline{x_m}\right)\left(1-\overline{x_0}\right)} \tag{10}$$

$$F_e=\frac{S\varepsilon\varepsilon_0 Q^2}{2(d-x)C_0} \tag{11}$$

Where $q=\frac{ma}{kd}$、$\overline{x}=\frac{x}{d}$、$p=\frac{F_e}{kd}$. The maximum value of the equilibrium position is:

$$\overline{x_m}=1-\sqrt{\frac{2p}{1-\overline{x_0}}} \tag{12}$$

Substituting this value into (10) can obtain the step signal critical value *qc*. When considering the parasitic capacitance of the TSV parallel connection, this value will be reflected in the C_0 term in (11). From the perspective of qualitative analysis, the introduction of the TSV parasitic capacitance will expand the critical range of step inertia forces or cause a larger equilibrium displacement under the same step inertia force.

Pulse signals are also limited in duration compared to step signals. Considering the initial conditions $V_0=a\Delta t$、$x_0=0.5a(\Delta t)^2$ at the end of the pulse and the reliable operating condition $E(X)-E(X)\ge 0.5ma^2(\Delta t)^2$, a dimensionless relationship can be obtained:

$$a(\Delta t)\le w_0 d\sqrt{\left(\overline{x}-\overline{x_0}\right)^2-2p\left(\frac{\overline{x}}{1-\overline{x}}-\frac{\overline{x_0}}{1-\overline{x_0}}\right)}\equiv w_0 df(p) \tag{13}$$

where w_0 is the signal frequency. The above formula is since the pulse amplitude is large, the duration is short, and the following discussion is required:

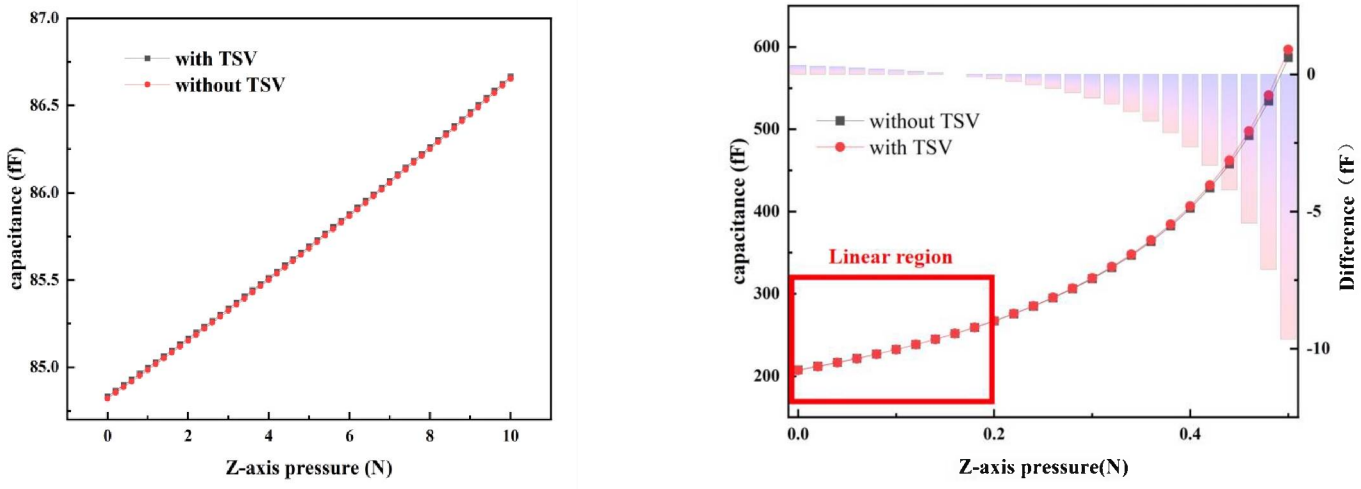
(1) During time Δt, the inertial force is much greater than the elastic force, the solution is $\Delta t<<\frac{\sqrt{2}}{w_0}$.

(2) At the end of the pulse, the inertial force is much greater than the damping force at the end of the pulse, and $\Delta t<<\frac{CV}{w_0}$ is solved currently.

After the above discussion, high frequency should be avoided as much as possible for the pulse force signal. The parallel parasitic capacitance introduced by TSV can improve the balance condition, which is mainly reflected in the relaxation of the pulse duration limit.

3. Simulation Results and Discussion

Fig. 6a shows the output results of the 150μm large cavity model, and its structural shape is consistent with Fig.4a-d. The sensitivity result is 0.1834fF/N regardless of whether TSV is present, and TSV brings a constant 0.011fF parasitic capacitance. This is because the linear range of the 150μm cavity is much larger than the impact of TSV and the change in parasitic capacitance is much smaller than the change in sensor sensitivity. Although the ground plate output mode is used, the parasitic effect is almost not reflected in the linear change. From the perspective of the excitation signal, the sensitivity is small, and the range is large, so the model has a relatively large introduction voltage and an equilibrium displacement larger than the material deformation range, and its data is not obvious enough in reliability simulations.



(a) (b)

Fig. 10. (a)150μm cavity model output. (b)Small cavity and difference change.

To amplify the changes introduced by TSV, the small cavity(10μm) model shown in Fig. 4a-d is used. Using this model can improve sensitivity without increasing structural complexity. Although the ratio of the plate to the cavity may introduce some edge effects, this effect can be ignored by selecting a reasonable linear interval for the degree of capacitance difference variation.

The large slope change in the small cavity model in Fig. 6b is due to the joint effect of the edge effect correction factor and the series and parallel parasitic capacitance. From the perspective of slope change, it can be proved that parasitic capacitance affects the linearity of the ground plate output mode. When the edge effect is avoided, this is easily reflected in the parasitic capacitance change caused by the voltage change of the TSV array. The measuring range of the small cavity model is 0.5N, and the slope change range between 0-0.16N does not exceed 0.5%. It can be posited that the range of 0.16N represents the linear range of the model, which is also consistent with one-third of the cavity range. From a stability perspective, it can be defined as a stable equilibrium displacement modulated by edge effects. When the linear range is not considered, the results in Fig. 6b show that TSV increases the system sensitivity by 19.96fF/N, and the maximum change increases by 2.63%.

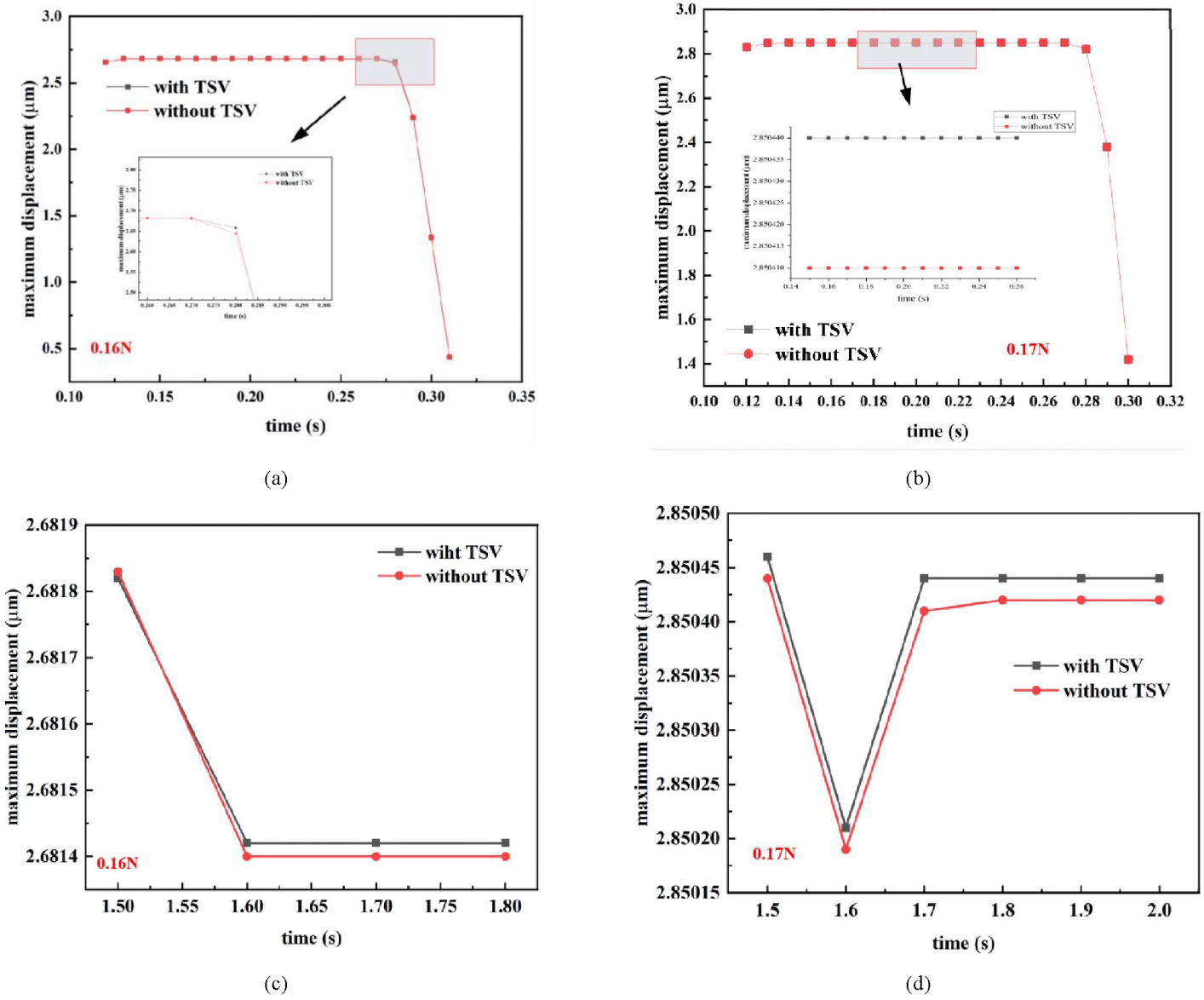


Fig. 7. (a) Maximum equilibrium displacement when pulse force (0.16N) is applied and falls back. (b)Maximum equilibrium displacement when pulse force (0.17N) is applied and falls back. (c)The maximum equilibrium displacement before and after the stable stage of step force (0.16N). (d) The maximum equilibrium displacement before and after the stable stage of step force (0.17N).

The excitation signal acts on the surface of the mass block at the top of the model (only applied in the Z-axis direction). Take 0.16N and 0.17N as the stable peak value and overtravel peak value of impulse force and step force.

There is basically no change in the trend of the pulse signal on the rising edge. Fig. 7a and Fig. 7b show the difference between the falling edge and the stable peak of the pulse signal:

(1) TSV makes the stable balance range larger.

(2) When the 0.16N pulse signal falls back, the existence of TSV slows down the maximum falling speed and improves the stability condition.

(3) When subjected to an over-travel pulse force (0.17N), the effect of TSV is relatively obvious in the maximum stable range, and the fallback speed is slightly slower than that of the model without TSV.

Before the step signal stabilizes, there will be a displacement overtravel beyond the final stable range. The difference shown in Fig. 7c and Fig. 7d can be expressed as: 1) When subjected to the critical step inertial force (0.16N), TSV reduces the displacement overtravel range and increases the stable balance range. 2) When subjected to an overtravel step inertia force (0.17N), the device will

have a vibration state before stabilizing. The existence of TSV expands the stable equilibrium range and improves the stable recovery rate.

The simulation results verified the predictions of the theoretical part, which means that the reliability of TSV under both excitation signals has been improved. This is a positive effect brought by parasitic capacitance, but it is not ideal for signal transmission. This situation also has the following aspects:

(1) While the use of small cavity models and multi-layer structures can enhance sensitivity, this approach is accompanied by increased process costs and a reduction in measurement range, which are both unfavorable outcomes.

(2) When using a large cavity model, the size of the TSV is usually much smaller than the MEMS sensor. Currently, the linearity of the output is hardly affected by the parasitic effects of TSV. However, the increase in system volume will increase the area waste of ASIC and the parasitic impact of metal interconnections.

(3) The design of coaxial ring columns and special TSV models can improve electrical isolation and stress problems, but the process difficulty increases significantly.

(4) As the TSV depth increases, the oxide layer thickness decreases, and the center distance decreases, the parasitic capacitance increases, thereby expanding the stable balance range and increasing the stable rate. However, the reduction in the thickness of the oxide layer will worsen the electrical isolation performance, and the reduction in the TSV center spacing will increase the stress.

4. Conclusions

In the study of the TSV model, the influence of size parameters on parasitic capacitance was determined, as well as the influence of parasitic effects caused by TSV shape. This article conducts relevant theoretical analysis and simulation verification on the influence trend of TSV basic parameters on parasitic capacitance, output mode, and reliability changes after bonding. In the study of the reliability of the force excitation signal, the maximum equilibrium displacement change caused by the parasitic capacitance introduced by TSV was deduced, and the influence of this small change was verified by simulating two cavity models of 150μm and 10μm, which is consistent with the changing trend of the theoretical analysis. A through hole with a diameter of 10μm (aspect ratio 2:1) can increase the sensitivity of a small cavity model by up to 2.63% (19.96fF/N). At the same time, the stable equilibrium range and recovery rate of the system are improved. The trade-off between process cost, performance, and size effects should be considered when designing and preparing MEMS-TSV integrated models for mass production.

The purpose of this study is to provide certain guidance and basic information for TSV-MEMS system integration rather than a perfect solution. If the negative impact is within an acceptable range, these trends can be used to optimize certain aspects of the product's performance to suit the use scenario. It should be emphasized that there are still some issues not mentioned here, such as the impact of shape and size on reliability and the issue of optimal ratios, which need further exploration.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Acknowledgement

This work was supported in part by the National Key R&D Program of China (No. 2022YFB3204800), the National Natural Science Foundation of China (No. U1909221 and No. 61871167), Zhejiang Provincial Talent Project(2021R52009).

References

[1] TAKATO, Minami, et al, Piezo impact type MEMS rotary actuator and application to millimeter size AI controlled robot, in Prague, Czech Republic. IEEE International Ultrasonics Symposium (IUS). 2013 201-204. https://doi.org/10.1109/ULTSYM.2013.0052.

[2] Makihata M, Tanaka S, Muroyama M, et al, Integration and packaging technology of MEMS-on-CMOS capacitive tactile sensor for robot application using thick BCB isolation layer and backside-grooved electrical connection, Sens. Actuator A Phys. 188 (2012) 103-110. https://doi.org/10.1016/j.sna.2012.04.032.

[3] Hoefflinger B. Chips 2020: a guide to the future of nanoelectronics. Berlin, Heidelberg: Springer Berlin Heidelberg, 2011.

[4] Fischer A C, Forsberg F, Lapisa M, et al, Integrating MEMS and ICs, Microsyst. Nanoeng. 1 (2015) 1-16. https://doi.org/10.1038/micronano.2015.5.

[5] Fischer, A C, et al, Unconventional applications of wire bonding create opportunities for microsystem integration, J Micromech Microeng. 2 (2013) 083001. https://doi.org/10.1088/0960-1317/23/8/083001.

[6] Davis W R, Wilson J, Mick S, et al, Demystifying 3D ICs: The Pros and Cons of Going Vertical, IEEE Des Test. 22 (2005) 498-510. https://doi.org/10.1109/MDT.2005.136.

[7] Tian J, Sosin S, Iannacci J, et al, RF-MEMS wafer-level packaging using through-wafer interconnect, Sens. Actuator A Phys. 142 (2008) 442-451. https://doi.org/10.1016/j.sna.2007.09.004.

[8] Wang, Zheyao, Microsystems using three-dimensional integration and TSV technologies: Fundamentals and applications, Microelectron Eng. 210 (2019): 35-64. https://doi.org/10.1016/j.mee.2019.03.009.

[9] Katti G, Stucchi M, De Meyer K, et al, Electrical Modeling and Characterization of Through Silicon via for Three-Dimensional ICs, IEEE Trans Electron Devices. 57 (2010) 256-262. https://doi.org/10.1109/TED.2009.2034508.

[10] Tsai M Y, Huang P S, Huang C Y, et al, Investigation on Cu TSV-Induced KOZ in Silicon Chips: Simulations and Experiments, IEEE Trans Electron Devices. 60 (2013) 2331-2337. https://doi.org/10.1109/TED.2013.2263298.

[11] Bryzek Janusz, Anthony Flannery, and David Skurnik, Integrating microelectromechanical systems with integrated circuits, IEEE Instrum Meas Mag. 7 (2004) 51-59. https://doi.org/10.1109/MIM.2004.1304566.

[12] Zhao W. S, et al, Frequency- and Temperature-Dependent Modeling of Coaxial Through-Silicon Vias for 3-D ICs, IEEE Trans Electron Devices. 58 (2011) 3358-3368. https://doi.org/10.1109/TED.2011.2162848.

[13] Su Jinrong, Fang Wang, and Wenmei Zhang, Capacitance expressions and electrical characterization of tapered through-silicon vias for 3-D ICs, IEEE Trans Compon Packaging Manuf Technol. 5(2015): 1488-1496. https://doi.org/10.1109/TCPMT.2015.2457938.

[14] Kim J, Pak J S, Cho J, et al, High-frequency scalable electrical model and analysis of a through silicon via (TSV), IEEE Trans Compon Packaging Manuf Technol. 1(2011) 181-195. https://doi.org/10.1109/TCPMT.2010.2101890.

[15] Ho S W, Rao V S, Khan O K N, et al, Development of coaxial shield via in silicon carrier for high frequency application, in Singapore.2006 8th Electronics Packaging Technology Conference. 2006 825-830. https://doi.org/10.1109/EPTC.2006.342819.

[16] Wang F, Yu N, An effective approach of improving electrical and thermo-mechanical reliabilities of through-silicon vias, IEEE Trans Device Mater Reliab. 17 (2017) 106-112. https://doi.org/10.1109/TDMR.2016.2626306.

[17] Hsieh M L, Yeh S K, Lee J H, et al, Vertically integrated multiple electrode design for sensitivity enhancement of CMOS-MEMS capacitive tactile sensor, in Berlin, Germany.20th International Conference on Solid-State Sensors, Actuators and Microsystems & Eurosensors XXXIII (TRANSDUCERS & EUROSENSORS XXXIII). 2019 2174-2177. https://doi.org/10.1109/TRANSDUCERS.2019.8808555.

[18] Bao M H. Micro mechanical transducers: pressure sensors, accelerometers and gyroscopes. Shanghai, China: Elsevier Science, 2000.

[19] Bao M H. Analysis and design principles of MEMS devices. Shanghai, China: Elsevier Science, 2005.