A COMPARATIVE STUDY OF ERROR-CORRECTING CODES FOR MULTI-CELL UPSETS IN MEMORIES: CLC AND OPCOSA

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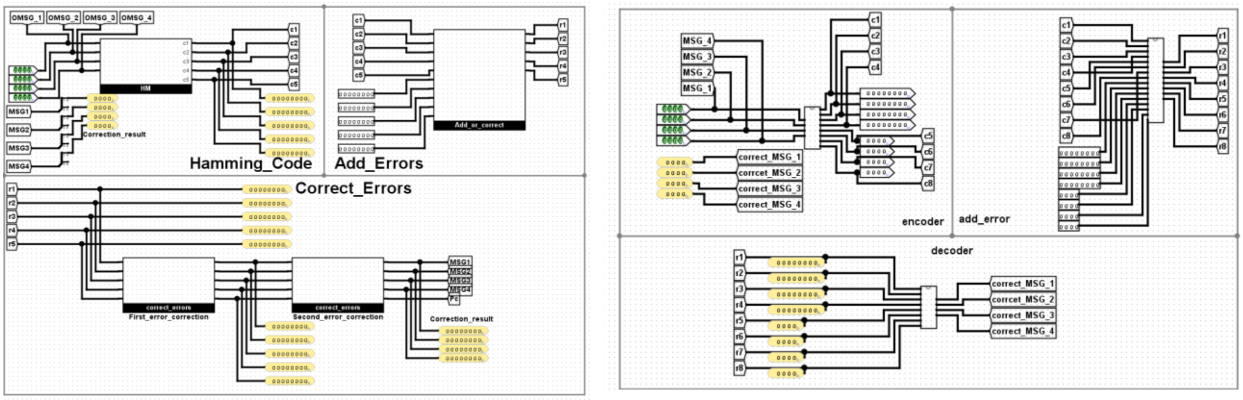
Annotation. With semiconductor scaling, memories are more vulnerable to radiation-induced Multiple Cell Upsets (MCU). This paper compares two 2D error-correcting codes: CLC and OPCoSA. It analyzes their coding structures and evaluates error correction ability, hardware overhead, and reliability via synthesis and fault injection. Experiments show CLC has moderate cost and decent performance. OPCoSA optimizes redundancy to cut hardware overhead while keeping strong correction. This study helps choose suitable ECCs for space memories under resource and reliability constraints.

Keywords. Matrix ECC, PCoSA, CLC and OPCoSA Algorithms.

Error Correction Code Principles and Structures: It is a two-dimensional matrix ECC that arranges data and redundant bits in rows and columns. Taking CLC (16,40) as an example, 16 data bits form a 4×4 matrix. An (8,4) extended Hamming code is applied row-wise to generate check and parity bits, and column parity is computed to form a 40-bit codeword [1]. This structure supports single-bit and multi-bit error correction. CLC includes variants (16,39) and (16,54) and supports Standard and Extended modes [2]. This work focuses on CLC (16,40).OPCoSA is an optimized product code derived from PCoSA [3, 4]. It arranges 16 data bits in a matrix and applies extended Hamming codes to both rows and columns to generate check and parity bits. Compared with PCoSA, OPCoSA removes the parity-on-parity region, shortening the codeword to 48 bits with 32 redundant bits, reducing redundancy by 33%. Although the minimum Hamming distance decreases to 7, the decoding algorithm still ensures strong MCU correction [3].

Experimental Setup: Hardware Implementation Gate-level circuits of CLC (16,40) and OPCoSA (48,16) are implemented in Logisim, including encoder, decoder, Hamming code modules, error injection, and correction output units. The results as show in Figures 1. Designs are then translated to Verilog and implemented on Xilinx Virtex-7 XC7V485TFFG1157-1 (28 nm CMOS) in Vivado.Error Correction Evaluation Fault injection is performed to simulate 1–8 adjacent errors to mimic MCU. Monte Carlo simulations are run for each pattern, and correction rates are counted under identical conditions for fairness.Hardware Overhead Metrics Overhead is evaluated using Vivado synthesis and power analysis:Resource utilization: Slice LUTs, registers, IOBs, BUFGCTRL, Power: total on-chip power, dynamic power, static power, Thermal parameters: junction temperature, thermal resistance, margin.



a *b*

Figure 1 – Gate - level circuit schematic of the algorithm: a – gate - level circuit implementation of CLC; b – gate - level circuit implementation of OPCoSA

Results and Discussion: Error Correction CapabilityBoth codes achieve 100% correction for 1–3 bit errors. At 4-bit errors, OPCoSA remains 100% while CLC drops to 48.69%. For 5-bit and 6-bit errors, OPCoSA reaches 53% and 35%, outperforming CLC (33.58%, 22.58%). OPCoSA supports full-codeword error correction, while CLC only corrects within information bits.Special Error Scenarios In ≤4-bit burst errors, OPCoSA corrects 100% vs. 75.5% for CLC. For >4-bit bursts, OPCoSA achieves 44% vs. 24% for CLC. In 36 typical space radiation patterns and 3×3 MCU mode, OPCoSA corrects 100% of errors, while CLC reaches only 75%–78%. Hardware Overhead CLC uses 752 LUTs, 251 registers, and 5.2 W. OPCoSA uses 1454 LUTs, 475 registers, and 7.6 W, approximately twice the overhead. The difference comes from longer codewords and more complex decoding. Experimental results as shown in Figures 2. and Figures 3.

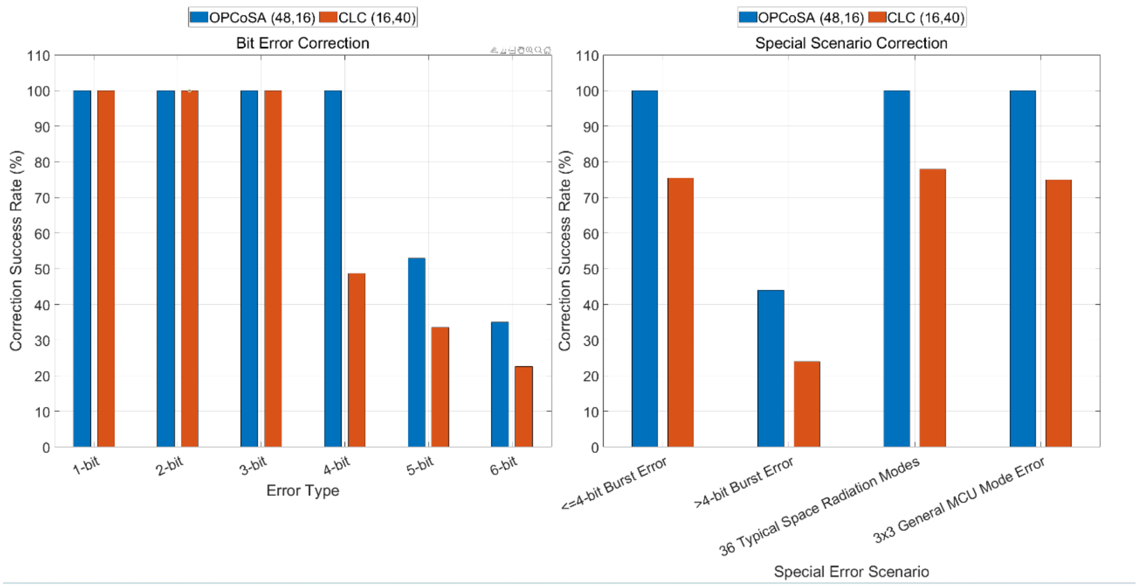


Figure 2 – Comparison of Error Correction Rates (%) Between CLC and OPCoSA Algorithms

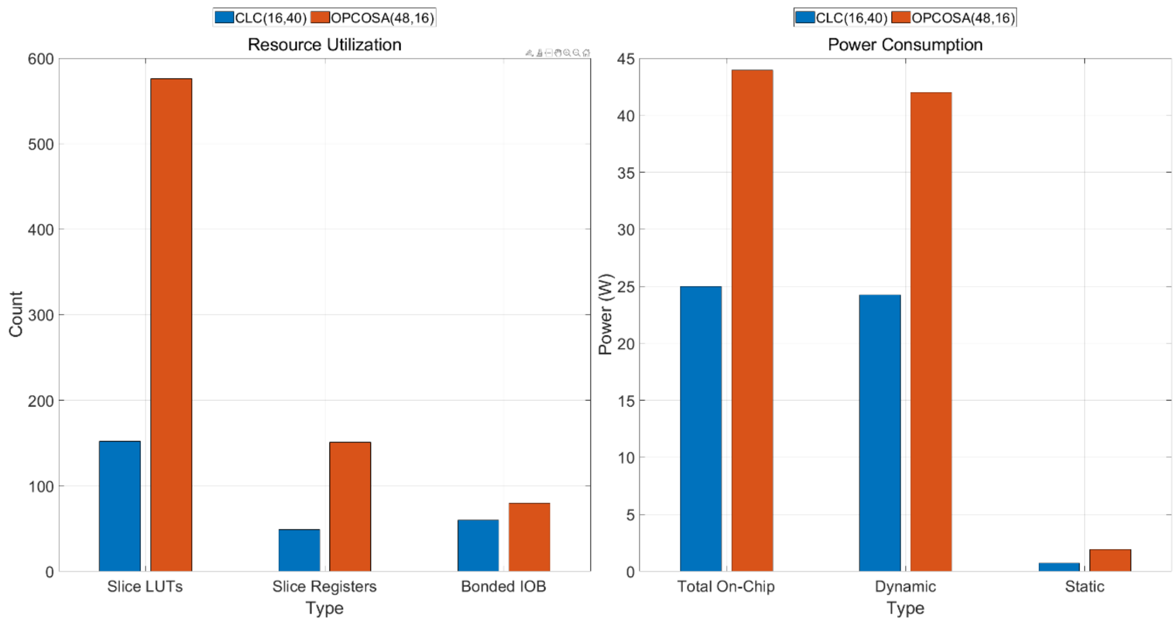


Figure 3 – Comparison of Hardware Overhead Between CLC and OPCoSA Algorithms

Conclusion: OPCoSA are both effective 2D ECCs for MCU mitigation. CLC provides low hardware cost and is suitable for resource-constrained systems with small MCU errors. OPCoSA delivers significantly stronger correction under 4-bit and complex multi-bit errors, supports full-codeword protection, and is more robust for high-reliability space applications despite higher overhead.Limitations include simplified fault injection, 28 nm FPGA only, and no voltage/temperature variation. Future work will extend evaluation to real radiation environments and advanced processes.

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