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THE FUTURE OF MICRO – AND NANOELECTRONICS

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Annotation. The article examines the future development of micro– and nanoelectronics in the context of the approaching physical and economic limits of Moore's Law. Key emerging technologies are analyzed, including two-dimensional materials (in particular InSe and 2D metals), neuromorphic computing, spintronics, three-dimensional heterogeneous integration (CFET, Forksheet) and advanced packaging solutions. The study highlights current challenges such as power consumption, heat dissipation and manufacturing scalability, while demonstrating how these innovations (including TSMC/Intel 2-nm processes 2025–2026 and wafer-scale InSe transistors) open new opportunities in artificial intelligence, quantum computing, energy-efficient systems and biomedical devices. It is shown that the transition to "beyond-CMOS" paradigms, supported by interdisciplinary research and international collaboration, will ensure transformative advances in electronics, increasing performance, sustainability and accessibility of next-generation devices.

Keywords: microelectronics, nanoelectronics, beyond Moore's Law, two-dimensional materials, neuromorphic computing, three-dimensional integration, spintronics, heterogeneous systems.

***Introduction*.** Micro– and nanoelectronics have been the cornerstone of technological progress for over five decades, powering everything from consumer devices to advanced computing systems. The exponential growth predicted by Moore's Law has driven unprecedented increases in transistor density, speed and energy efficiency. However, as device dimensions approach the atomic scale, traditional silicon-based CMOS technology is encountering fundamental physical limits, including quantum tunneling, heat dissipation and skyrocketing manufacturing costs [1]. Modern research is shifting toward "More-than-Moore" and "beyond-CMOS" paradigms that integrate novel materials, architectures and functionalities to sustain innovation [2]. This article explores the future trajectory of micro– and nanoelectronics, focusing on emerging technologies, their applications and the prospects for overcoming current barriers.

Main part. One of the primary challenges facing conventional microelectronics is the slowing of Moore's Law scaling [1]. At nodes below 3 nm, issues such as leakage current, parameter variability and thermal management become critical. In 2025–2026, leading companies such as TSMC and Intel are launching mass production of 2-nm (TSMC N2) and 20A/18A (Intel, 1.8 nm) processes. TSMC's N2 process utilizes gate-all-around (GAA) nanosheet transistors and delivers up to 15 % higher performance and 30 % lower power consumption compared to the 3-nm node, while Intel's 18A process introduces RibbonFET GAA transistors combined with PowerVia backside power delivery technology, reducing interconnect resistance by 30 % and improving energy efficiency by 25 % [4]. At the same time, research institutes (imec, CEA-Leti) are actively testing CFET (complementary FET) and Forksheet architectures. In CFET, n– and p-type transistors are stacked vertically with a common gate, achieving a 2× increase in transistor density at a 25 nm gate pitch. Forksheet technology adds dielectric isolation between n– and p-channels, further reducing parasitic capacitance and enabling sub-1 nm effective channel lengths [2].

To overcome these fundamental limits, researchers are intensively studying alternative materials and device concepts. Two-dimensional (2D) materials such as graphene, transition metal dichalcogenides (TMDs – MoS_2, WS_2), black phosphorus and especially the new "golden semiconductor" InSe possess atomic thickness (single layer ~0.7 nm), exceptional carrier mobility and a tunable bandgap (0.3–2.0 eV depending on layer number). In August 2025, a team from Peking University successfully fabricated the first 2-inch wafer-scale InSe films using metal-organic chemical vapor deposition (MOCVD). The resulting transistors demonstrated electron mobility of 287 $cm^2/V \cdot s$, a subthreshold swing of only 67 mV/dec and an energy-delay product already surpassing the IRDS 2037 roadmap targets for silicon [6]. In addition, the synthesis of the first true 2D metals (bismuth, tin, lead, indium, gallium) with a record thickness of 6.3 Å was recognized as

the Physics World 2025 Breakthrough of the Year. These 2D metals enable zero-Schottky-barrier contacts, eliminating a major source of contact resistance in ultra-scaled devices [7].

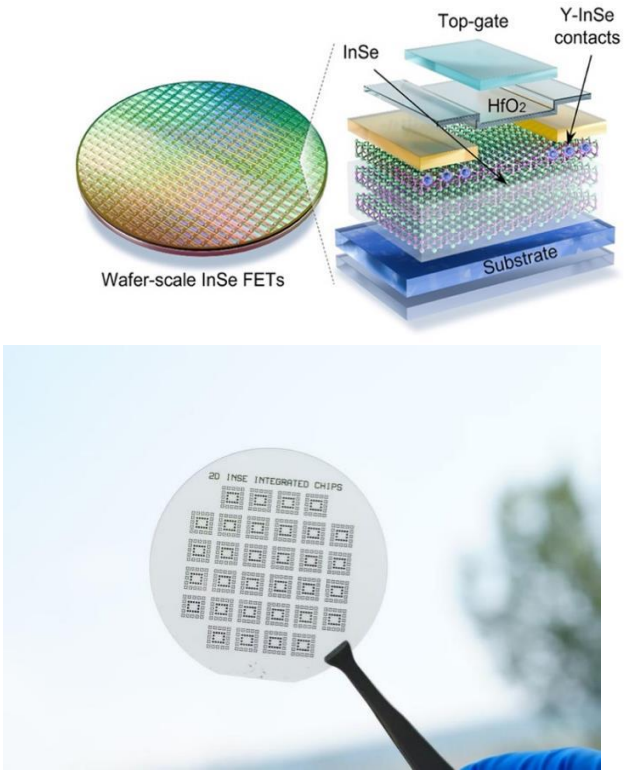

Figure 1 – Wafer-scale 2D InSe transistors (Peking University, 2025)

Another rapidly developing direction is neuromorphic computing, which emulates the architecture and principles of the human brain to achieve ultra-low-power information processing. Modern neuromorphic systems use 2D-material-based memristors, 3D crossbar arrays and photon-avalanching nanoparticles developed at Berkeley Lab (2025). These components enable true in-memory computing, eliminating the von Neumann bottleneck of constant data shuttling between memory and processor. For example, a 3D neuromorphic chip with 1 million memristive synapses can perform 10^{12} operations per second per watt – three orders of magnitude more energy-efficient than conventional GPUs [3]. Such solutions are especially promising for edge-AI applications in IoT devices, autonomous systems and biomedical implants, where power budget is limited to microwatts.

Spintronics represents a separate breakthrough area, using electron spin rather than charge for data storage and processing. Spin-transfer torque magnetic RAM (STT-MRAM) and spin-orbit torque (SOT) devices already demonstrate non-volatile operation, write energy below 1 pJ/bit and endurance exceeding 10^{15} cycles. Samsung and TSMC have integrated STT-MRAM into 7 nm and below processes for last-level cache, while hybrid CMOS-spintronic circuits allow simultaneous logic and memory functions with power dissipation reduced by 70 % compared to SRAM [5].

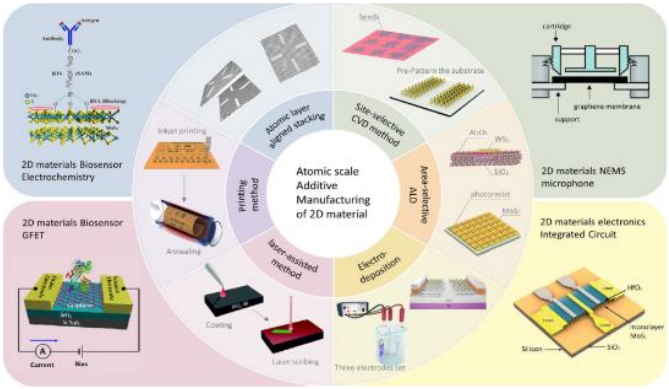

Figure 3 – 3D heterogeneous chip integration (DARPA and industry developments 2025)

The general scheme of future micro– and nanoelectronics development can be represented as a multi-stage process: from materials discovery and device prototyping through system-level integration and packaging to application-specific optimization and large-scale manufacturing.

Regarding the future prospects of micro– and nanoelectronics, the integration of advanced materials and architectures is still evolving, yet the potential is immense. As fabrication technologies mature, several key advancements are anticipated:

1 AI-Driven Design and Optimization: Machine learning algorithms will accelerate the discovery of new materials and circuit topologies, enabling rapid prototyping of custom devices tailored to specific applications.

2 Quantum and Neuromorphic Hybrid Systems: Combining classical nanoelectronics with quantum bits and brain-like processors will unlock unprecedented computational capabilities for complex simulations and AI training.

3 Sustainable and Low-Power Electronics: Focus on energy-harvesting nanomaterials and recyclable 2D devices will reduce the environmental footprint of electronics manufacturing and operation.

4 Biomedical and IoT Integration: Nanoelectronic sensors and implantable devices will enable real-time health monitoring and personalized medicine, while ultra-low-power chips will power the next wave of ubiquitous IoT networks.

***Conclusion*.** Thus, the future of micro– and nanoelectronics lies in overcoming the limitations of traditional scaling through innovative materials, architectures and integration strategies. Thanks to the introduction of two-dimensional materials (InSe, 2D metals), neuromorphic and spintronic devices, as well as advanced three-dimensional packaging technologies (CFET, 3D stacking), the industry is ready to offer more powerful, efficient and sustainable electronic systems. These achievements will not only ensure further technological progress but also open new horizons in computing, healthcare, energy and communications. Continued investment in research infrastructure, interdisciplinary collaboration and workforce training will be the key condition for realizing the full potential of nanoelectronics and maintaining global leadership in this critically important area.

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