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DESIGN OF 2.4 – 2.5 GHz RECEIVER WITH AUTOMATIC GAIN CONTROL SYSTEM

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Annotation. This paper presents the design of Radio Frequency Receiver with Automatic Gain Control System. The integrated AGC system increased the receiver's dynamic power range on 15 dBm. The frequency range of 2,4 – 2,5 GHz finds application in RFID chips, in IoT devices and in modern wireless network systems, such as Wi-Fi, Bluetooth and others.

Keywords: radio frequency RF, wireless communication, integrated receiver, AGC system

Introduction. Incredible improvement of wireless technologies stimulates enhancing of RF receivers to establish the fastest and the reliable data transformation. In a common radio environment, a receiver must handle a massive range of signal strengths, typically spanning 70 dBm to over 100 dBm of variation. This factor requires feedback system, which corrects gain depending on the level of input signal. This part can be implemented by Automatic Gain Control (AGC) system. The system extends dynamic range of receiver by adjusting gain of LNA so, that sensitivity of the system is maximized in case of absence of interference in receive channel, while if interferer is there, AGC improves systems linearity.

This paper presents the design and simulation of integrated RF receiver with AGC system including its operation in situation of frequently changing signals.

The typical architecture of receiver block. Next, the design and performance of receiver is discussed. The typical architecture of receiver is presented in Figure 1.

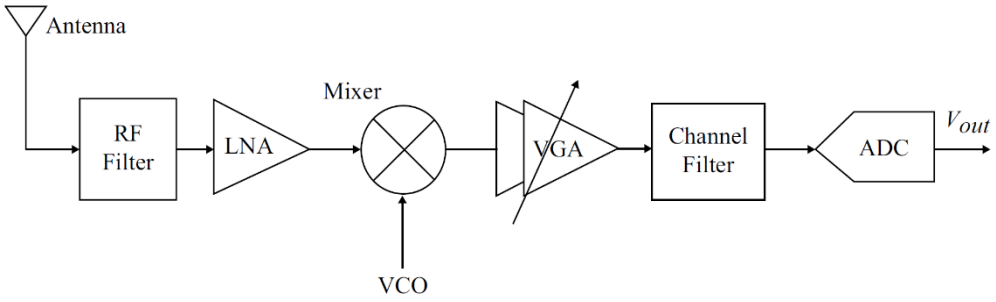


Figure 1.1 – The typical architecture of receiver [1]

This is a superheterodyne receiver architecture, which was invented decades ago, is still the most popular architecture in modern RF receivers [2]. It includes Antenna, RF Filter, Low-Noise Amplifier (LNA), Mixer, Automatic Gain Control System (it can be implemented as Variable Gain Amplifier), Channel Filter and Analog-to-Digital Converter (ADC). In this paper we will concentrate on three of them: LNA, Mixer and AGC system.

Low Noise Amplifier. The role of LNA is to boost the received signal a sufficient level above the noise floor so that it can be used for additional processing [3]. This block is the first of the receiver and therefore its Noise Figure (NF) directly limits the sensitivity of the receiver. NF is a relative parameter, which shows the degradation of Signal to Noise Ratio (SNR) after its passing through the electric block. In radio terms, if a signal is weaker than the noise floor, it is effectively lost, regardless of how much gain you add later. Also, the linearity of LNA is essential, because it defines the LNA's ability to handle strong signals without distortion.

The impact of LNA as the first cascade, may be demonstrated by the "Friis' equation". According to it, the noise contributed by each stage decreases as the total gain preceding that stage

increases, implying that the first few stages in a cascade are the most critical [4]. It can be calculated by the formula:

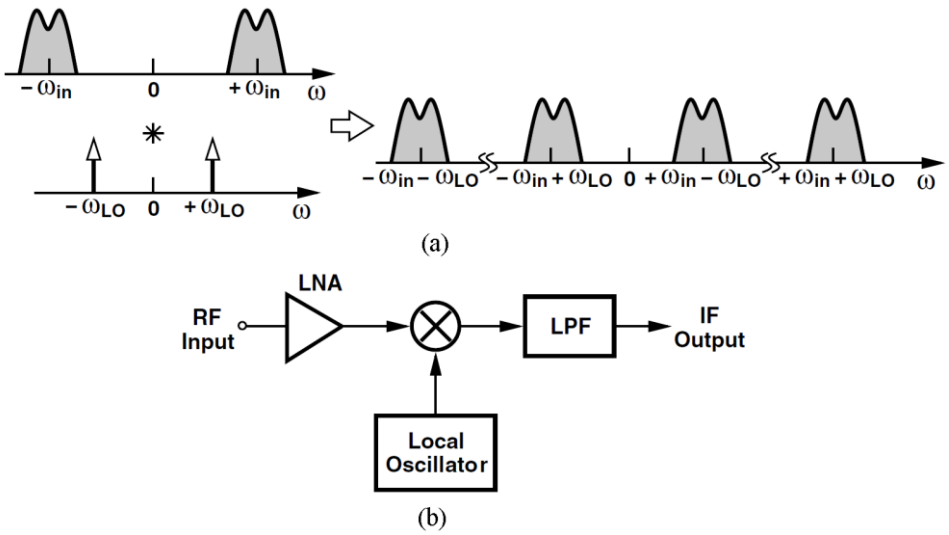
$$NF_{tot} = 1 + (NF_1 - 1) + \frac{NF_2 - 1}{A_{P1}} + \cdots + \frac{NF_m - 1}{A_{P1} \cdots A_{P(m-1)}}, \quad (1.1)$$

where *NF* – Noise Figure, which represents the level of the block;

A_P – Gain of the block.

This equation suggests, that the LNA affects other blocks of the receiver. Conversely, if a stage suffers from attenuation (loss), then the NF of the following circuits is "amplified" when referred to the input of that stage [4]. In other words, as every block increases the overall gain, noise and distortions of the signal are also amplified and affect the performance of the system. That's why the parameters of LNA as the first block of the receiver are so essential. However, the Design of an LNA typically consists of trade-off between Noise Figure (NF) and Gain while designing at the required stability.

Mixer. If we are talking about wireless communications, the transferred data signals usually lie in Radio Frequency (RF) range. However, it is technically difficult and expensive to design blocks that operate in this range (mostly in GHz). So, converting the signal to a lower Intermediate Frequency (IF) allows more efficient and stable processing. For this purpose, downconversion mixer is usually used, which main role is to perform frequency translation by multiplying input signal with so called LO signal, usually generated by local on-chip oscillator (the oscillator is out of scope of our discussion). Due to multiplication of signals with different frequencies, we get two combinations with sum and difference of two frequencies (Figure 1.2(a)). The components at $\pm(\omega_{in} + \omega_{LO})$ are not of interest and are removed by the low-pass filter (LPF), leaving the signal at a center frequency of $\omega_{in} - \omega_{LO}$. This operation is called "downconversion mixing" or simply "downconversion." Due to its high noise, the downconversion mixer is preceded by a low-noise amplifier (Figure 1.2 (b)).



(a) – resulting spectra after conversion; (b) – The "Conversion block"

Figure 1.2 – The performance of downconversion mixer [4]

In receiver design, the mixer acts as a "bridge" between the high-frequency signals and lower-frequency processing stages. So, its performance directly dictates the sensitivity and linearity of the entire system. Because the Mixer typically follows the LNA, which provides significant gain, it is usually exposed to much higher power levels, making it the primary bottleneck for intermodulation distortion. This statement represents by the next formula [4]:

$$\frac{1}{{A_{IP3}}^2} \approx \frac{1}{{A_{IP3,1}}^2} + \frac{{A_{P1}}^2}{{A_{IP3,2}}^2}, \quad (1.2)$$

where A_{IP3} – linearity of the specific block;

A_{P1} – gain of the LNA.

So, the equation (1.2) suggests, that the gain of LNA affects the signal level seen by Mixer at input and thus its linearity, which limits linearity of the whole system. So, because the mixer is the bottleneck for linearity, improving mixer's IP3 (interception point on 3 dB) is the only way to maintain high dynamic range without sacrificing receiver's linearity.

***Automatic Gain Control system*.** The AGC block is responsible for varying the gain due to input signal, forming the feedback loop.

The AGC function can mainly be implemented in two different ways according to the signal which senses the amplitude and adjusts the gain correspondingly. If the input VGA signal is used, the AGC loop moves forward in the receiver signal direction, so this loop is called "feedforward loop". On the other hand, if the output VGA signal is sensed, the AGC loop moves backwards in the signal direction. This loop is called "feedback loop". Both structures are drawn in Figure 1.3. Between both loop structures, the feedback one is the most popular when designing AGCs since it provides higher linearity and requires narrower dynamic range (DR) in the detector [1].

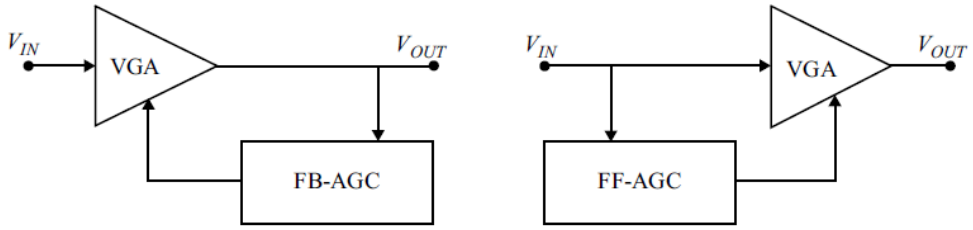


Figure 1.3 – Feedback and Feedforward AGC architectures [1]

In a receiver, an Automatic Gain Control (AGC) block is essential for maintaining a stable output signal despite wide fluctuations in the strength of the incoming radio signal. Without it, the output (such as audio volume) would constantly change as you tune to different stations or as environmental conditions fluctuate. When a strong signal is received, AGC reduces the gain to prevent internal circuits from saturating or «clipping», which would otherwise cause harsh distortion.

For weak signals, AGC increases gain to boost them above the receiver's internal noise floor, ensuring clear reception.

The performance of the AGC system can be described in the following steps. Detector stage (Power Detector, PD) monitors the average or peak strength of the signal at the output. Then it generates a DC control voltage proportional to the signal's strength. And finally, this voltage is fed back to earlier LNA stage to automatically increase or decrease their gain as needed.

***The design of the receiver*.** This chapter represents the design of the receiver. Technical specification of the receiver is presented in Table 2.1.

Table 2.1 – Technical specification of the project

Parameter	**Value**	**Units**
Voltage supply (V_{dd})	1,8	V
Frequency operation range	2,4 – 2,5	GHz
Central frequency	2,45	GHz
Intermediate frequency (IF)	1	MHz
Maximum gain	20	dB
Current consumption	≤ 10	mA
IIP3 (linearity)	≥ −10	dBm
Noise Figure (system)	≤ 8	dB
Noise Figure (LNA)	≤ 2	dB
AGC bit depth	3 (8 steps)	bit

The proposed design of the receiver is presented in Figure 2.1. Actually, this system is divided into four blocks: Power Detector, Low-Pass Filter, Comparator Block and AGC Block. The performance of the majority of blocks was described higher. Here we will concentrate on the AGC and Comparator blocks.

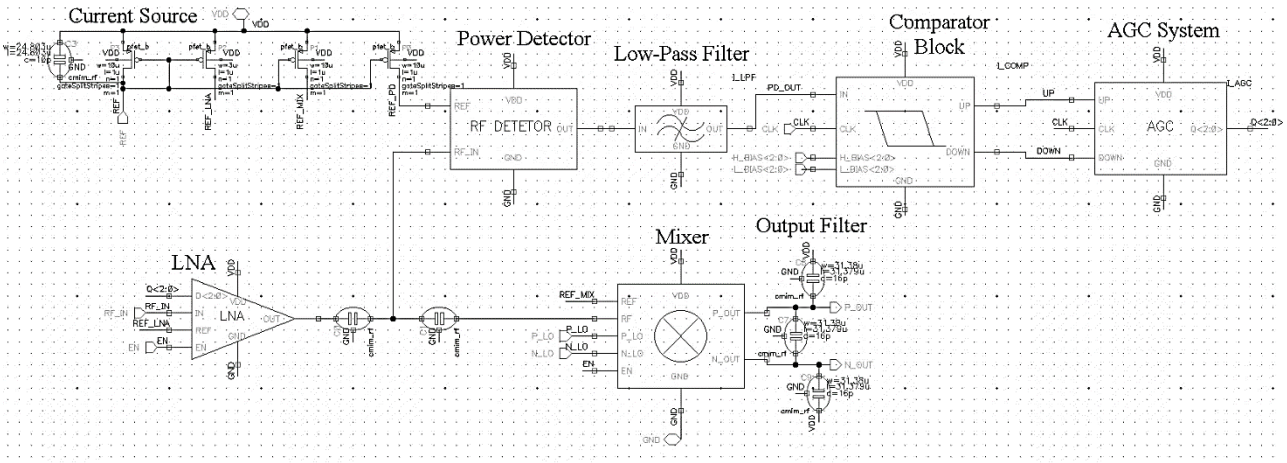


Figure 2.1 – The proposed design of receiver

The comparator block forms two output signals according to the result of comparison: if signal is higher than programmed threshold, it creates “DOWN” signal, if too small – “UP” signal. And finally, the AGC system creates 3-bit digital code, which manipulates the LNA’s gain. At the beginning of operating digital code is “000” what corresponds to the smallest gain. And then with each clock cycle the system either changes the digital code or keeps it unchanged.

The parameters of the simulation are following. Frequency of the output signal is 5 MHz and the clock’s frequency is 10 MHz. During the simulation the input signal is changing from –50 dBm to −30 dBm with step of 5 dBm every 500 ns. It’s essential to simulate the dynamic changing input signal, which often occurs in real use cases.

The results of TRAN-analysis are presented in Figure 2.2. Here we can see the response of the receiver to dynamically changing input signal. Depending on the output power detector’s signal “PD_OUT”, there is changing of the digital code from outputs Q0 – Q2. If the detector’s signal lower than low threshold, the comparator block generates the “UP” signal, during which the LNA’s gain is increasing until the maxim value “111”. When the signal is between two thresholds, the gain value keeps the same. And when the detector’s output signal reaches the high threshold, the gain of amplifier starts decreasing.

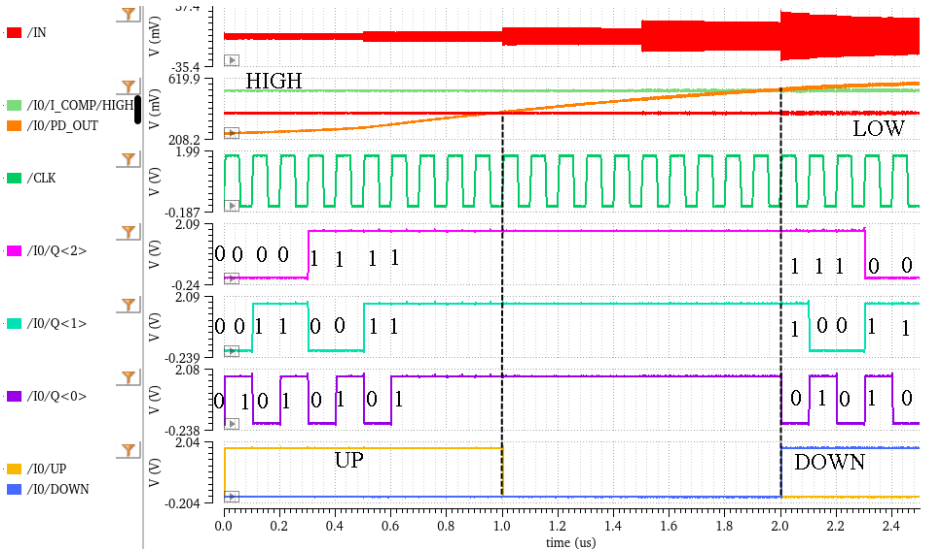


Figure 2.2 – The results of TRAN-analysis

To make sure, that amplifier’s gain is really changing, we can look at the output signal, which is presented in Figure 2.3.

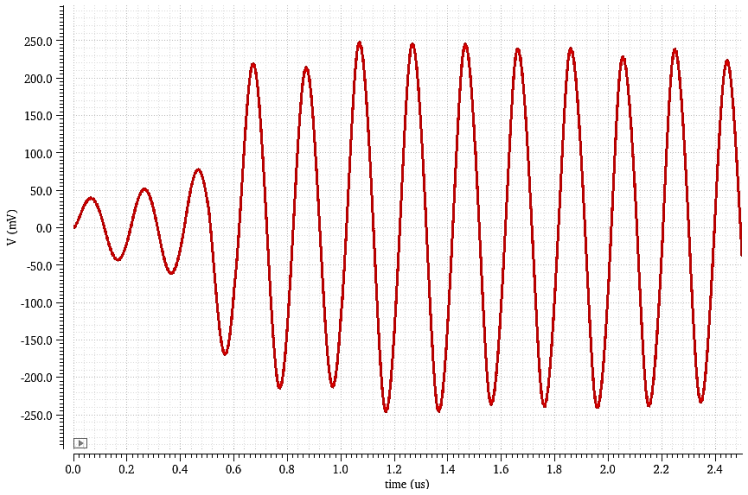


Figure 2.3 – The output signal of the receiver system

In this figure we can see changing of the output signal. Before 500 ns the output signal is changing with LNA's gain. Then the signal is increasing due to the higher input signal and at some moment it's stabilized. So, according to Figures 5 and 6 we can conclude, that the receiver's AGC block operates correctly.

The parameters of the receiver are presented in Table 2.2 (the analysis of corners isn't included).

Table 2.2 – Parameters of the receiver

Parameter	**Value**		**Units**
	min	**max**	
Gain	5,5	20,14	dB
Current consumption	10,6	10,8	mA
IIP3 (system)	− 31(high gain)	− 9,15 (low gain)	dBm
IIP3 (LNA)	− 22,4 (high gain)	− 13,5 (low gain)	dBm
Noise Figure (system)	5,5 (high gain)	7,5 (low gain)	dB
Noise Figure (LNA)	1,82 (high gain)	1,86 (high gain)	dB

According to table 2.2 we can conclude, that the receiver operates as desired and the dynamic power range was enhanced on 15 dBm, because the difference between maximum and minimum gains is about 15 dB.

Conclusion. This paper provided design of the receiver with AGC system. The main difference between our design and the classic superheterodyne receiver architecture is that instead of VGA Block we used LNA with variable gain, what improves the linearity of the receiver system.

The performance of the receiver in dynamic conditions was analyzed. LNA's gain is increasing when it's lower than low threshold, decreasing when the signal is over the high threshold and don't change when it's between two of threshold. According to the results, we can conclude, that the receiver system and AGC Block are operating correctly and that due to AGC system the dynamic range of the receiver was increased.

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