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SPECIFICS OF PARAMETRIC MEASUREMENT OF SEMICONDUCTOR DEVICES USING VERILOG-A

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Abstract: the article examines the specifics of parametric modeling for semiconductor devices using the Verilog-A analog description language. It highlights the main drawbacks of standard SPICE libraries, such as fixed parameter sets, limited adaptability to new component types, and the difficulty of accounting for nonlinear temperature and time dependencies in semiconductor structure characteristics. The stages of constructing a parametric model are described: identifying physical control parameters, formulating a system of analytical equations, replacing fixed coefficients with variables, and final verification against experimental data.

Keywords: parametric modeling, semiconductor devices, Verilog-A, SPICE, computer simulation, nonlinear characteristics.

1. INTRODUCTION: CHALLENGES OF SEMICONDUCTOR DEVICE SIMULATION IN MODERN MICROELECTRONICS

1.1. Limitations of Traditional SPICE Modeling for Modern EDA and Circuit Design

The ongoing evolution of microelectronics, integrated circuit miniaturization, and automated electronic design workflows imposes growing requirements on modern EDA tools and semiconductor device simulation methodologies. Traditional circuit simulation workflows based on standard SPICE model libraries remain widely adopted in industrial CAD systems; however, they exhibit critical limitations that restrict their applicability for advanced analog and mixed-signal circuit design. Conventional SPICE models operate on fixed template structures with static parameter sets, offering limited flexibility for adapting to new semiconductor architectures, updated fabrication processes, and complex nonlinear operating conditions.

A major drawback of template-based SPICE modeling is its inability to dynamically account for temperature drift, frequency-dependent effects, time-based aging degradation, and batch-specific device variations. In modern microelectronics design, where high integration density, low-power operation, and extreme environmental tolerance are mandatory, fixed SPICE libraries often produce significant simulation inaccuracies. These discrepancies negatively affect the entire EDA design pipeline, including circuit schematic verification, transient analysis, parametric optimization, and final prototype validation.

To resolve these modeling limitations within automated design workflows, flexible user-defined modeling techniques have become essential for contemporary EDA practice. The Verilog-A analog hardware description language provides a powerful solution for customizable parametric modeling, fully compatible with modern CAD environments. It enables engineers to construct physical-level device descriptions based on analytical equations rather than predefined templates, significantly improving the accuracy and adaptability of circuit simulation throughout the electronic design automation process.

Parametric modeling via Verilog-A defines semiconductor device behavior through fully configurable mathematical relationships governed by geometric, physical, and operational parameters. This methodology supports iterative model updating, precise environmental dependency adjustment, and custom calibration – all essential capabilities for robust automated analog circuit design in modern EDA systems.

Semiconductor components including diodes, bipolar and field-effect transistors, sensors, and photovoltaic cells demonstrate highly nonlinear current–voltage characteristics sensitive to temperature, supply voltage, operating frequency, and material aging. Standard SPICE models rely on averaged manufacturer parameters and cannot capture device-specific nonlinear behaviors or non-standard physical effects. In contrast, Verilog-A parametric descriptions allow full adjustment of structural geometry, temperature coefficients, load response characteristics, and batch-level calibration, greatly enhancing the reliability of EDA simulation results.

The accuracy of parametric device modeling directly determines the stability of automated design workflows, the quality of circuit optimization, and the efficiency of microelectronic device prototyping. By embedding customizable physical models into EDA tools, designers minimize reliance on generic library components and achieve higher consistency between simulation predictions and real hardware performance.

As a flexible high-level modeling language for analog and mixed-signal systems, Verilog-A fundamentally extends the modeling capability of conventional EDA platforms. Unlike rigid SPICE templates, Verilog-A supports complete mathematical definition of internal physical processes, enabling full parameterization of conductance values, threshold voltages, leakage characteristics, and temperature dependencies. All core device parameters can be modified independently without full code rewriting, which streamlines iterative design refinement in automated circuit development pipelines.

Furthermore, Verilog-A supports complex nonlinear differential equations suitable for describing transient responses, junction charge dynamics, and frequency-dependent component behaviors. Custom Verilog-A models can be seamlessly integrated into mainstream EDA frameworks to supplement or replace outdated SPICE libraries, making them indispensable for designing newly developed semiconductor devices that lack standardized industrial models. The extendable structure of Verilog-A code also facilitates the implementation of environmental dependency models, including temperature fluctuation effects, humidity influence, power supply variation, and long-term structural degradation — key factors for reliable automated circuit validation. The development of complete Verilog-A parametric models follows a standardized workflow compatible with modern EDA design procedures. First, critical physical parameters are defined according to device type, including resistance, leakage current, breakdown voltage, threshold characteristics, sensitivity, and power generation parameters. Second, analytical physical equations are constructed to describe electrical behavior under varying operating conditions, replacing fixed SPICE coefficients with adjustable parametric variables. Finally, completed models are verified through DC analysis, AC frequency response testing, and multi-temperature sweep simulation, with parameter calibration performed by comparing simulated data with experimental measurements.

Compared with conventional SPICE-based design flows, Verilog-A parametric modeling eliminates template constraints and allows full customization of nonlinear and transient physical characteristics. Although custom model development requires additional initial effort, it significantly improves simulation precision and expands the capability boundary of automated analog circuit design, making it highly valuable for advanced microelectronics research and industrial EDA applications.

In engineering practice, Verilog-A parametric modeling enhances multiple automated design tasks: high-precision analog circuit design, low-power photovoltaic system optimization, smart sensor network modeling, transistor switching characteristic tuning, and multi-condition reliability prediction. By improving simulation accuracy within EDA workflows, the methodology reduces physical prototype testing costs, shortens design cycles, and supports multi-variant numerical analysis for circuit performance optimization.

1.2. Software tools supporting Verilog-A for circuit simulation

Modern EDA ecosystem includes both commercial and open-source simulation platforms capable of integrating Verilog-A custom models into automated circuit design pipelines. Popular open-source simulation suites, such as gEDA with ngspice or gnucap backends and QUCS, provide partial Verilog-A support through the ADMS compilation framework. Verilog-A behavioral descriptions are automatically translated into compilable C code and integrated with simulator core modules, enabling open-source customization of device models for academic and low-budget industrial EDA research.

Full commercial EDA platforms, including Cadence and Mentor Graphics environments, provide native Verilog-A compilation and simulation support; however, proprietary licensing limits their accessibility for educational and independent research projects. Alternatively, lightweight multi-platform simulation tools such as Dolphin SMASH and SymicaDE support hybrid SPICE and Verilog-A modeling workflows suitable for mixed-signal automated design. SymicaDE, in particular, offers comprehensive compatibility with Verilog, Verilog-AMS, VHDL, VHDL-AMS, and standard SPICE netlists, enabling unified multi-language EDA simulation across Windows and Linux operating systems

In summary, parametric modeling of semiconductor devices using Verilog-A serves as a vital, high-precision tool in modern scientific research and the engineering design of microelectronic devices. This approach overcomes the inherent limitations of standard SPICE models, allows for the specific accounting of physical and operational parameters, and accurately simulates complex dynamic processes within semiconductor structures. Its configuration flexibility, adaptability, and high mathematical precision drive the demand for Verilog-A in engineering practice and the development of next-generation electronic systems. Future advancements in parametric modeling methodologies using this language aim to create universal, adaptive, next-generation models suitable for a broad range of semiconductor devices. Despite its flexible multi-

language support for automated circuit modeling, SymicaDE presents certain limitations in professional EDA workflows. Its error reporting system is less detailed compared with industrial-grade Cadence Spectre simulation tools, occasionally causing unstable program behavior on outdated or non-native Linux distributions. The inconsistency of cross-platform performance restricts its large-scale industrial deployment, though it remains an effective lightweight solution for academic Verilog-A modeling research and small-scale automated circuit verification.

CONCLUSION

In modern electronic design automation and microelectronics engineering, Verilog-A parametric device modeling represents an advanced and high-precision simulation methodology capable of overcoming the structural limitations of traditional SPICE libraries. By enabling fully customizable physical-level descriptions of semiconductor devices, Verilog-A significantly improves the accuracy, flexibility, and scalability of analog and mixed-signal circuit simulation within standard EDA design pipelines.

The presented modeling approach supports adaptive parameter tuning, multi-environmental condition analysis, and custom nonlinear effect characterization, which are essential for designing miniaturized, high-precision, and reliable modern microelectronic systems. Although custom Verilog-A model development involves increased modeling complexity, its advantages in simulation accuracy and design flexibility substantially optimize automated circuit verification and performance prediction workflows.

Future research will focus on developing universal adaptive Verilog-A modeling frameworks compatible with mainstream EDA tools, aiming to establish standardized parametric modeling solutions for emerging semiconductor devices and next-generation automated circuit design systems.

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СПЕЦИФИКА ПАРАМЕТРИЧЕСКОГО ИЗМЕРЕНИЯ ПОЛУПРОВОДНИКОВЫХ ПРИБОРОВ С ИСПОЛЬЗОВАНИЕМ VERILOG-A

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Аннотация: в статье рассматриваются особенности параметрического моделирования полупроводниковых приборов с использованием языка аналогового описания Verilog-A. Освещаются основные недостатки стандартных библиотек SPICE, такие как фиксированные наборы параметров, ограниченная адаптивность к новым типам компонентов и трудности при учете нелинейных температурных и временных зависимостей характеристик полупроводниковых структур. Описаны этапы построения параметрической модели: физическая идентификация управляющих параметров, формулирование системы аналитических уравнений, замена фиксированных коэффициентов переменными и заключительная верификация на основе экспериментальных данных.

Ключевые слова: параметрическое моделирование, полупроводниковые приборы, Verilog-A, SPICE, компьютерное моделирование, нелинейные характеристики.