A STUDY ON LINEAR REGRESSION OF CPI AND MISS RATIOS IN HIERARCHY MEMORY OF NEHALEM SYSTEMS

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Recently, with growing the gap between processors and memory speeds, parallel performance on chip multithread processors becomes more attractive for filling up this gap. It occurs the multithread scheduling on chip multithread processors to improve the performance. In this direction, calculating the Cycle per Instructions (CPI) and its relationship with miss ratios in hierarchy memory is important. To finding the correlation between CPI and miss ratios and footprints, it's required to show linear relation between them at first. In this paper, linear regression between CPI and miss ratios has discussed in hierarchy memory including Translation Look-aside Buffer (TLB), first level of cache (L1), L2 and L3 on a Nehalem system. Intel-Vtune 2013 and SPEC-CPU 2000 benchmarks are used to measure the CPI and cache miss ratios.

The parallel processing is a way to filling up the gap between processors and memory speeds. Increasing the performance and scheduling the threads is required to calculate the Cycle per Instruction (CPI) and miss ratios in hierarchy memory including Translation Look-aside Buffer (TLB), first level of cache (L1), L2 and L3.
Looking the footprints on hierarchy memory and its correlation is nee to calculate the CPI. In this way, it is necessary to know the linear relation between CPI and hierarchy memory components at first.

Intel-Vtune 2003 and SPEC-CPU 2000 are tools to calculating the CPI and miss ratios of caches. Tables 1 and Table 2 show respectively: system specification to test and events used. The following benchmarks are used: BZIP2, CRAFTY, EON, GAP, GCC, GZIP, MCF, PARSER, PERLBMK, TWOLF, VORTEX and VPR. Each benchmark has ruined 50 times and 3 phases. Totally, 1800 phase-run performed.

Table 1.The properties of system under test

CPU	Core		L1 cache				L2 cache		L3 cache	
			Size		Descriptor					
	Main	Threads	Instruction	Data	Instruction	Data	Size	Descriptor	Size	Descriptor
Intel(R) Core(TM) i5 2.53 GHz	2	4	32KByte * 2	32KByte * 2	4-way set associative, 64 line size	8-way set associative, 64 line size	256Kbyte * 2	8-way set associative, 64 line size	3 Byte (Shared)	12-way set associative, 64 line size

Table 2.Hardware events and its descriptions used by Intel-Vtune 2013.

	Event Name		*Description Event*
1	CPU_CLK_UNHALTED.THREAD	6	L2_DATA_RQSTS.ANY
2	INST_RETIRED.ANY	7	MEM_LOAD_RETIRED.L2_HIT
3	L1D_ALL_REF.ANY	8	MEM_LOAD_RETIRED.LLC_MISS
4	L1I.CYCLES_STALLED	9	MEM_LOAD_RETIRED.LLC_UNSH_HIT
5	L1I.READS	10,11	SNOOP_RESPONSE.HIT, HITM

The linear regression between CPI and miss ratios for all benchmarks shows the linear relation between them. The figure 1a to 1d shows the linear regression with its equations on GZIP benchmarks as an example. In this example, 1, 5466 is the slope of line between CPI and all miss ratios.

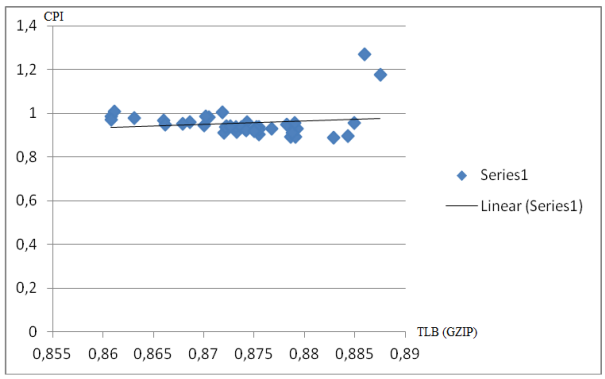

Figure 1a.The relation between CPI and TLB miss on GZIP, Slope line is 1.5466

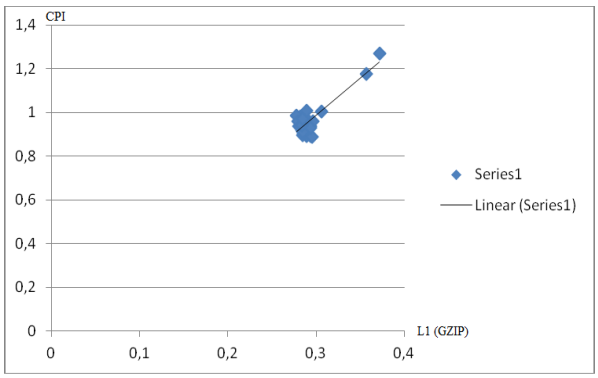

Figure 1b.The relation between CPI and L1 miss on GZIP, Slope line is 3.397

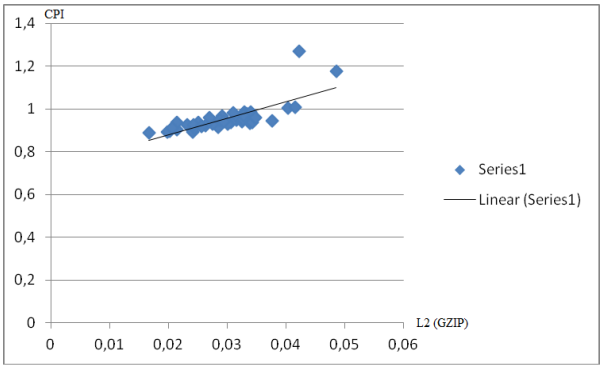

Figure 1c.The relation between CPI and L2 miss on GZIP,

Slope line is 7.802

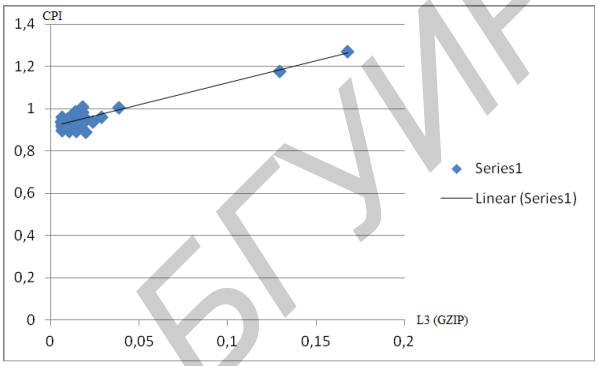

Figure 1d.The relation between CPI and L3 miss on

Slope line is 2.0881

The Table 3 shows all slope of linear regression on 12 benchmarks. As we can see, most coefficients are positive and most of them are negative.

Table 3.The slopes of linear regression

Benchmark	TLB	L1	L2	L3
GZIP	1,5466	3,397	7,802	2,0881
MCF	6.2804	4.5119	-6.8716	3.5388
CRAFTY	-0,2787	2,8778	9,8282	1,6934
GAP	1,6898	2,324	6,8227	3,0343
PARSER	4,7128	3,5606	-3,909	2,1581
TWOLF	24,704	5,0532	-6,3722	3,1272
VORTEX	6,2804	4,5119	-6,8716	3,5388
BZIP2	115.08	14.062	116.3	100.86
VPR	-392.95	-19.269	-359.12	208.92
PERLBMK	9.634	3.0752	141.37	19.183
GCC	-9.3687	-0.2181	-12.042	-160.41
EON	-0,5441	1,8927	-17,901	8,8025

The study on 12 integer benchmark of SPEC-CPU 2000 with Intel-Vtune 2013 shows the relation between CPI and miss ratios on the Intel Core i5, 2.53 GHz as a Nehalem system. This relationship in some cases is positive and in some cases is negative. Moreover, in some cases the value of the slope of lines is large and in some cases is small. This means that, performance impact of different Benchmarks on memory hierarchy is different.

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